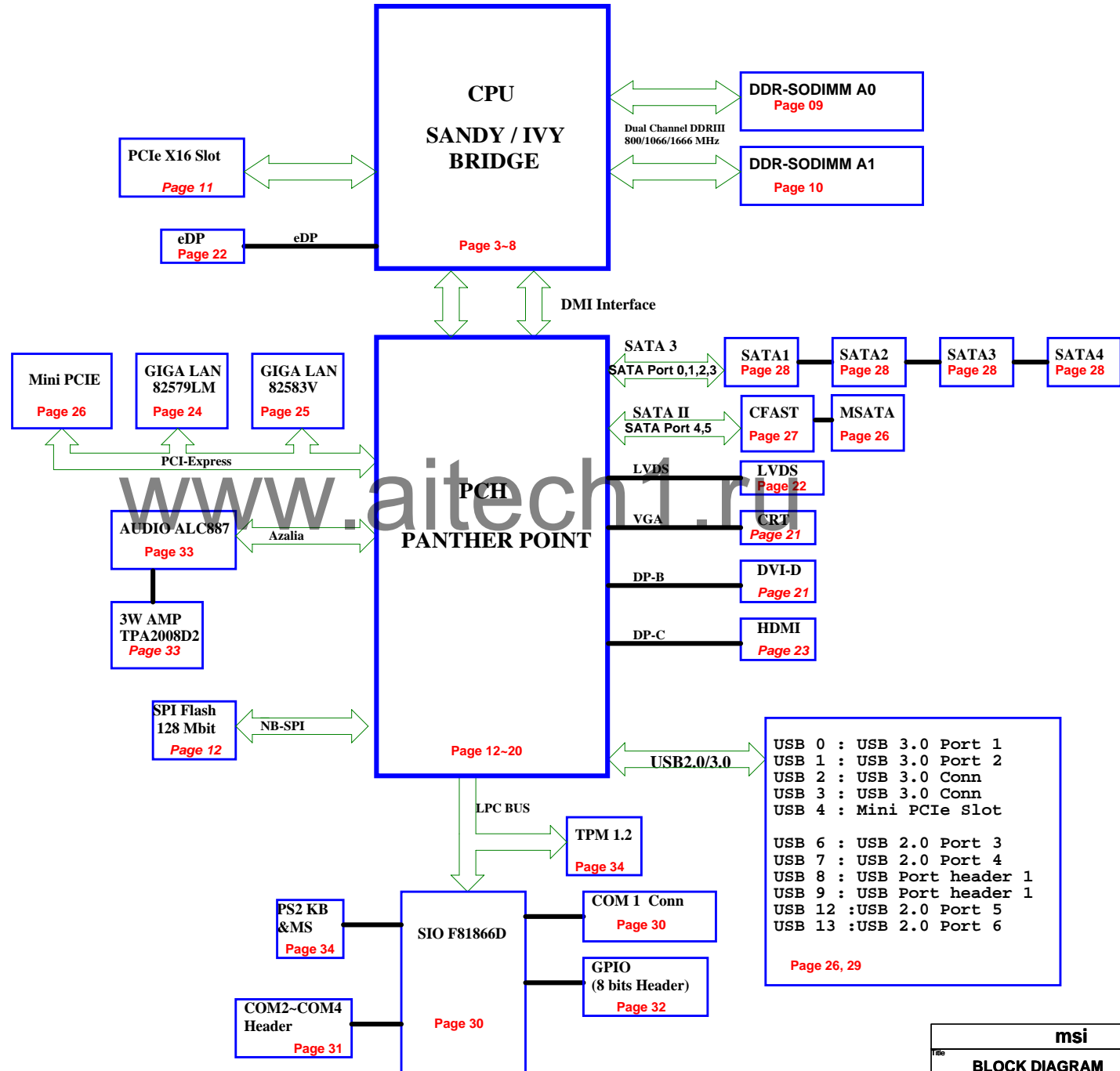


Chief River Platform

- 01 : BLOCK DIAGRAM
- 02 : PLATFORM
- 03 : PROCESSOR-1 (HOST BUS)
- 04 : PROCESSOR-2 (DDR3)
- 05 : PROCESSOR-3 (POWER)
- 06 : PROCESSOR-4 (GRAPHICS POWER)
- 07 : PROCESSOR-5 (GND)
- 08 : PROCESSOR-6 (RESERVE)
- 09 : DDR3 SODIMM A0
- 10 : DDR3 SODIMM A1
- 11 : PCI Express X16 Slot
- 12 : PCH-1 (HDA/JTAG/SATA)
- 13 : PCH-2 (PCI-E/SMBUS/CLK)
- 14 : PCH-3 (DMI/FDI/GPIO)
- 15 : PCH-4 (LVDS/DDI)
- 16 : PCH-5 (PCI/USB/NVRAM)
- 17 : PCH-6 (GPIO/NCTF/RSVD)
- 18 : PCH-7 (POWER)
- 19 : PCH-8 (POWER)
- 20 : PCH-9 (GND)
- 21 : VGA, DVI
- 22 : LVDS & EDP Connector
- 23 : HDMI-LEVELSHIFT
- 24 : LAN 82579LM & iAMT Power
- 25 : PCIE LAN (82583V)
- 26 : USB 3.0 & Mini PCie Slot
- 27 : CFAST
- 28 : SATA, FAN
- 29 : USB2.0 Conn
- 30 : SIO(F81866D)
- 31 : COM PORT
- 32 : GPIO Conn
- 33 : Audio ALC887
- 34 : FRONT PANEL,PS/2,TPM
- 35 : ATX & DSW POWER
- 36 : DDRIII 1.5V_DIMM
- 37 : VTT_CORE
- 38 : IMPV7- ISL95836HR (3+2Phase)
- 39 : IMVP7 Driver ISL6208BCRZ
- 40 : CPU_SA POWER/ 1.05VM_LAN
- 41 : Power Controller
- 42 : Screw, EMI, BOM-Option Parts
- 43 : Power MAP
- 44 : GPIO PIN Definitions/confige
- 45 : PWROK MAP/CLOCK MAP
- 46 : SIO GPIO PIN Definition
- 47 : History



SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

Voltage Rails

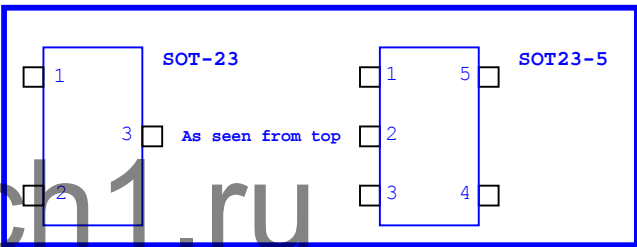
POWER PLANE	VOLTAGE	ACTIVE IN	DESCRIPTION
+12V	12V	S0	
-12V	-12V	S0	
VCC5	5V	S0	
VCC3	3V	S0	
+1_5VDIMM	1.5V	S0,(S3-S4)	
+1_5VRUN	1.5V	S0	
+0_75VRUN	0.75V	S0	
+V1_05M_LAN	1.05V	S0,(S3-S5)	
+VTT_CORE	1.05V	S0	
+V1_05M	1.05V	S0,(S3-S5)	
+1_8VRUN	1.8V	S0	
+0_85VRUN	0.85V	S0	
+VCC_CORE	1.05V-1.1V	S0	
3VSB_DS	3.3V	S0,(S3-S5)	
5VSB_DS	5V	S0,(S3-S5)	
3VSB	3.3V	S0,(S3-S5)	
5VSB	5V	S0,(S3-S5)	

Net Naming Conventions

Suffix
= Active Low Signal

Prefix
H = Host
M = DDR Memory
TP = Test Point (does not connect anywhere else)

PCB Footprints



Power States

	SLP S3#	SLP S4#	SLP S5#	+V*ALWAYS	+V*SUS	+V*RUN	CLK
S0 (Full on)	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft Off)	LOW	LOW	LOW	ON	OFF	OFF	OFF

msi

Title

PLATFORM

Size

Custom

Document Number

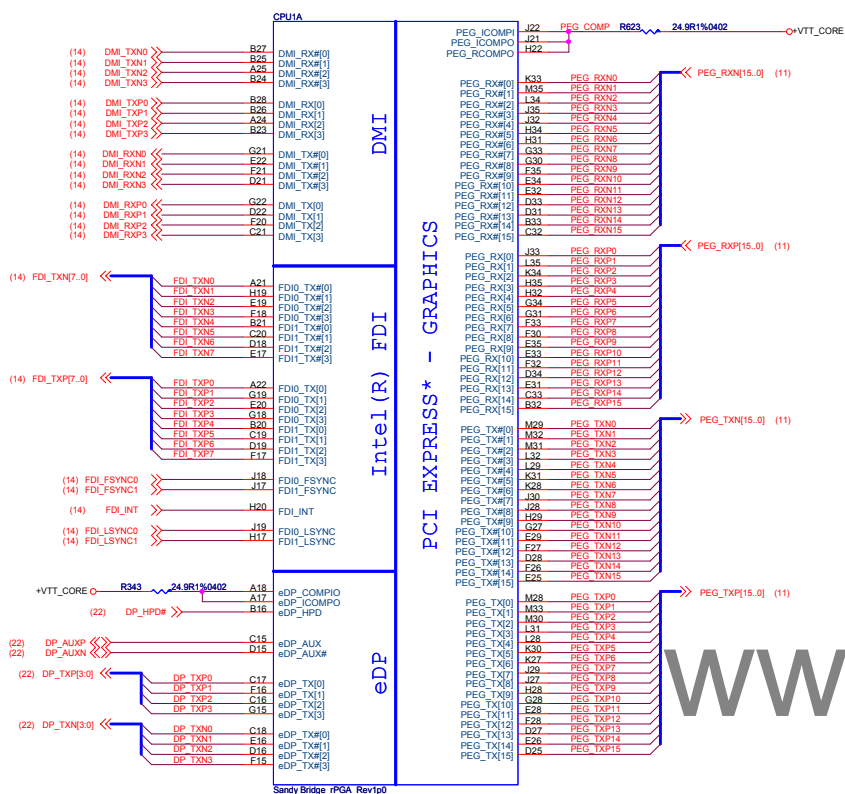
Rev

10

Date: Tuesday, July 31, 2012

Sheet 2 of 47

IVYBRIDGE PROCESSOR (CLK,MISC,JTAG)

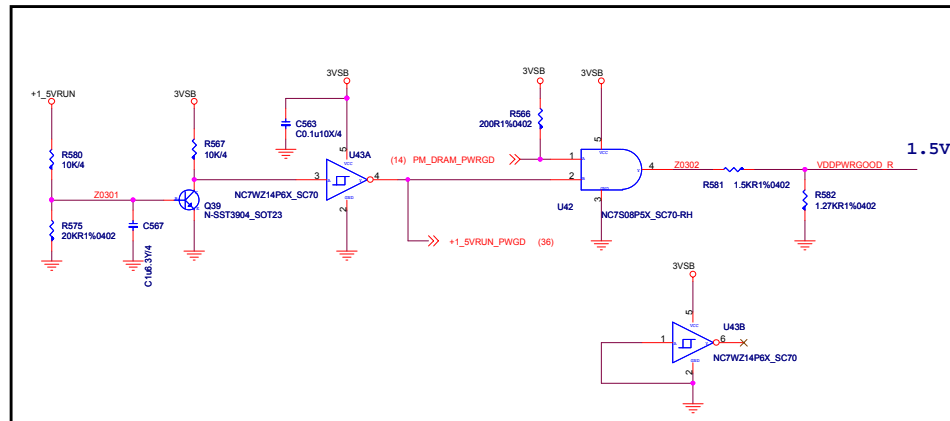
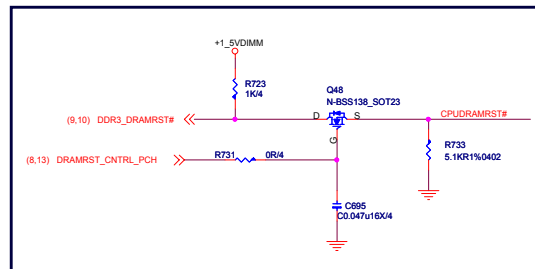


eDP_COMPIO
Width:4mils Spacing:15mils

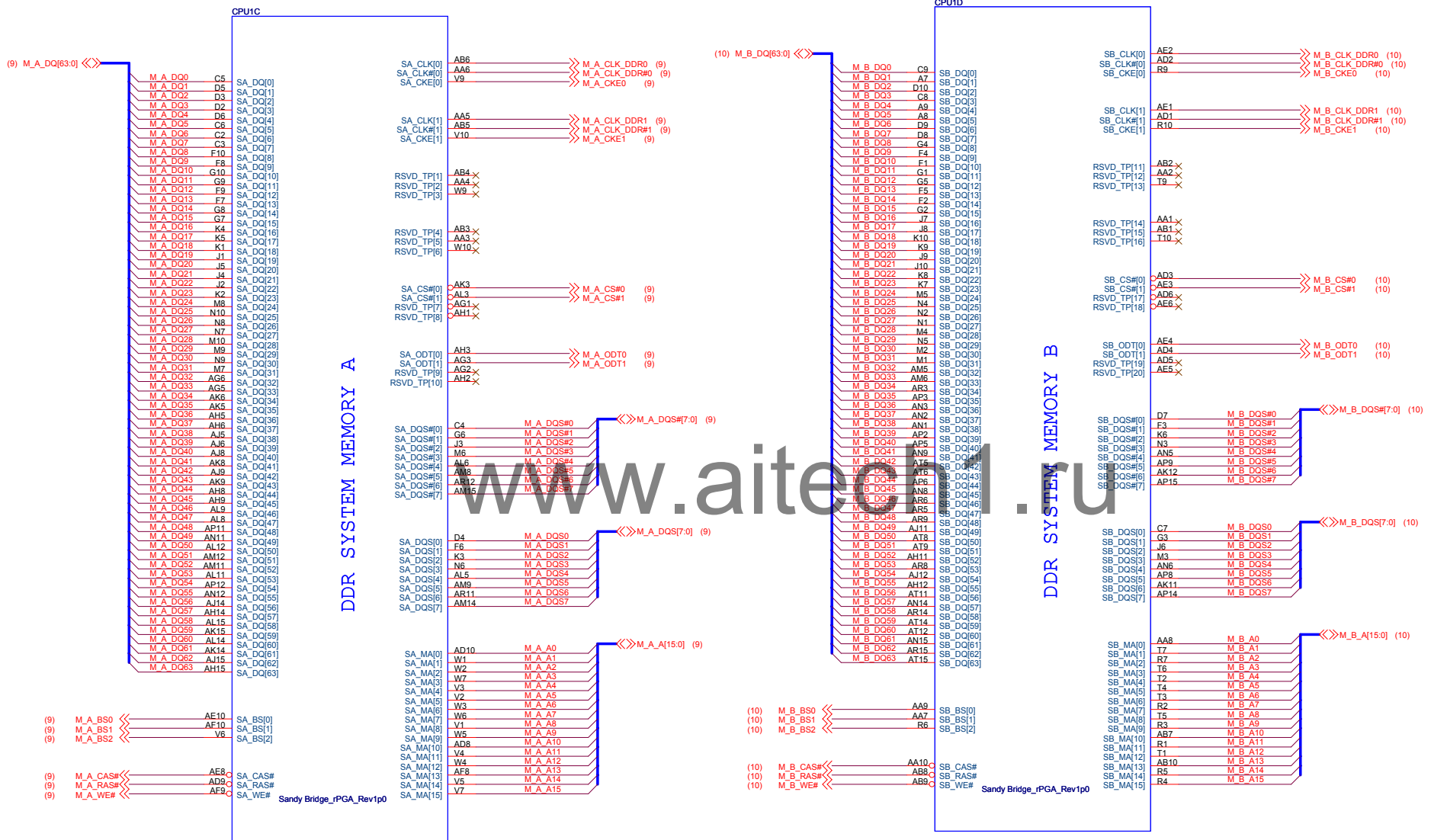
eDP_ICOMPO
Width:12mils Spacing:15mils

eDP_COMPIO,eDP_ICOMPO Length max: 500mil

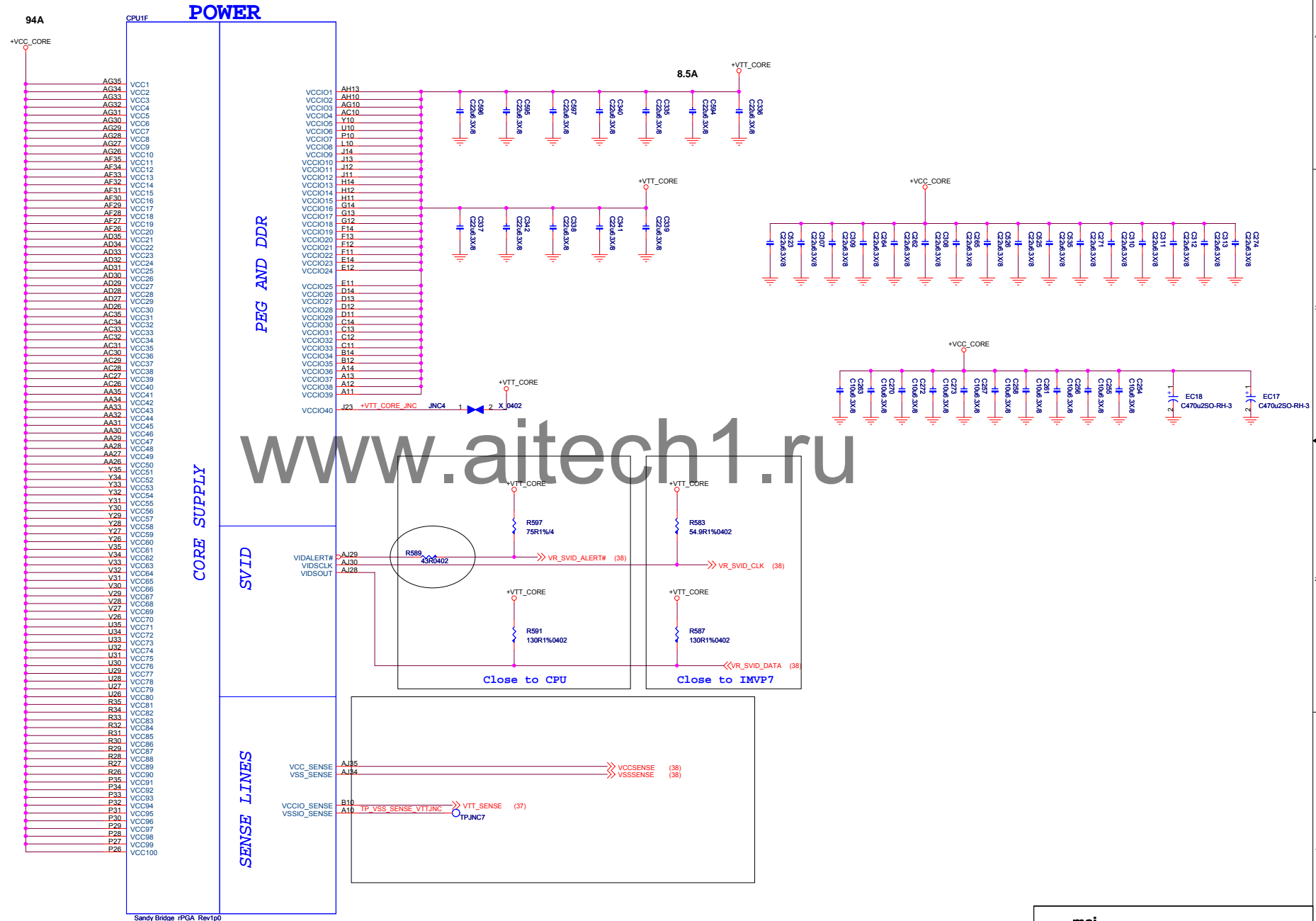
Intel Comments:
eDP COMP signals are required
if integrated gfx is enabled even
if eDP interface is disabled.



IVYBRIDGE PROCESSOR (DDR3)

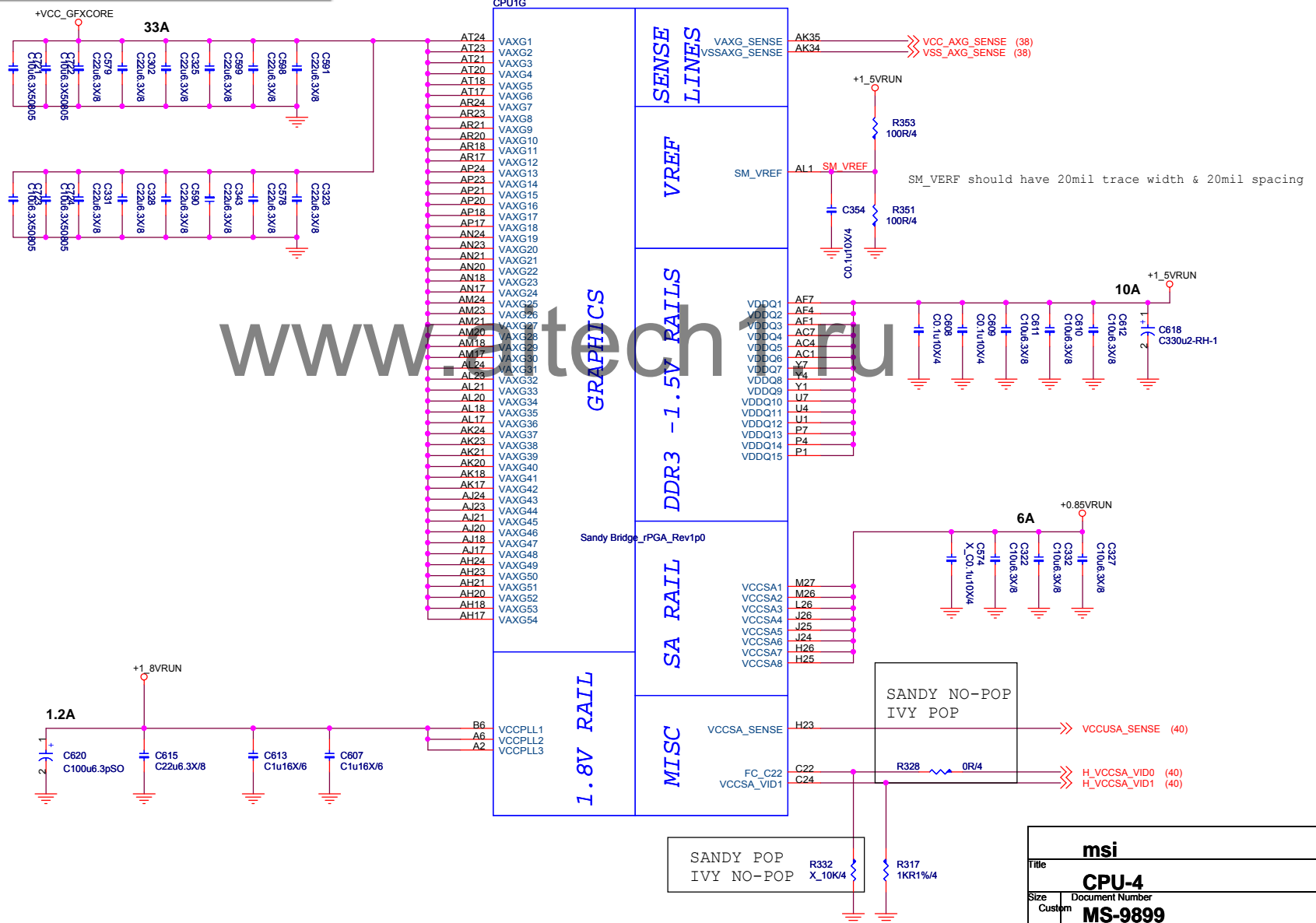


IVYBRIDGE PROCESSOR (POWER)

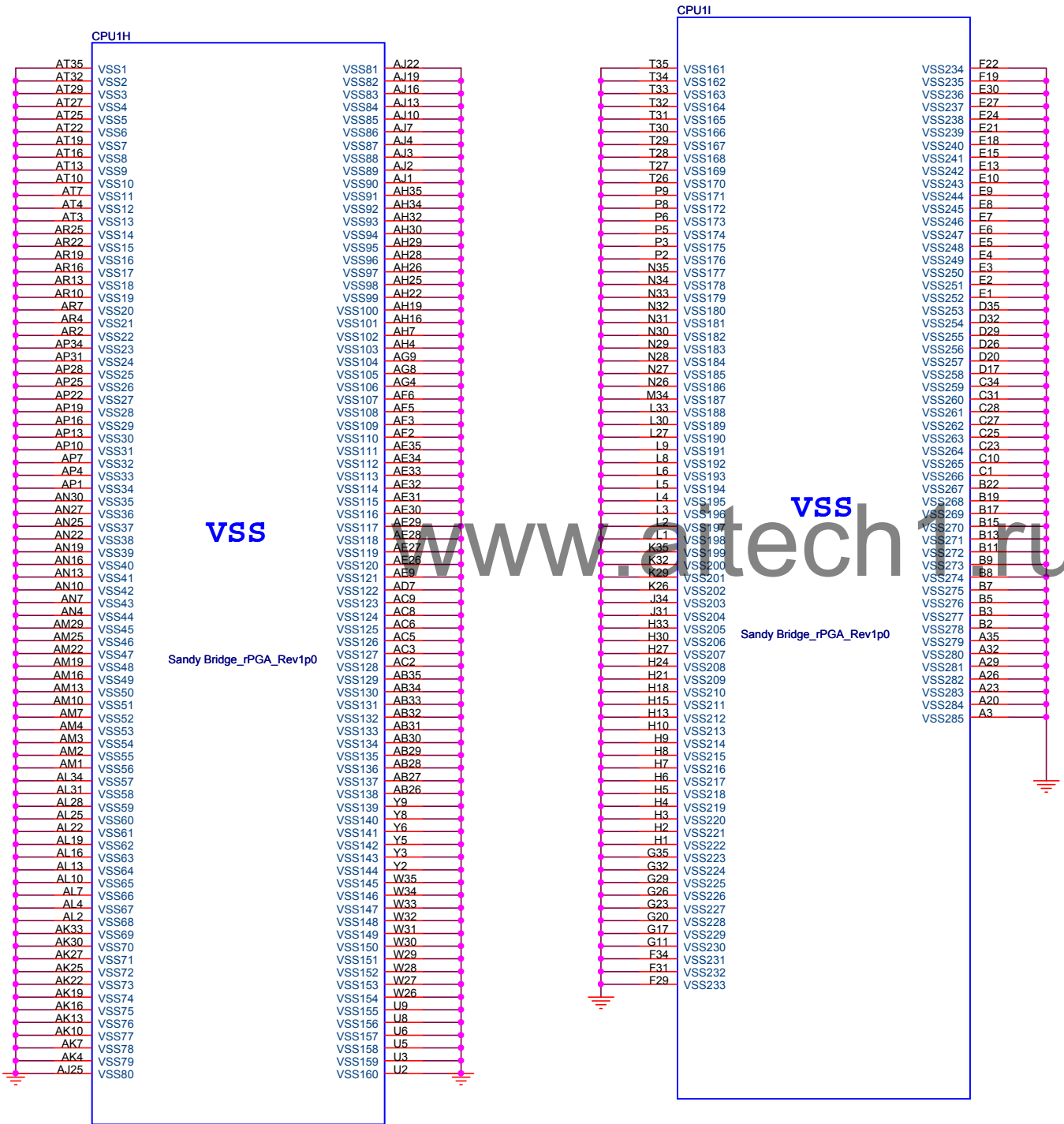


VCCSA_SEL Voltage Selection Table

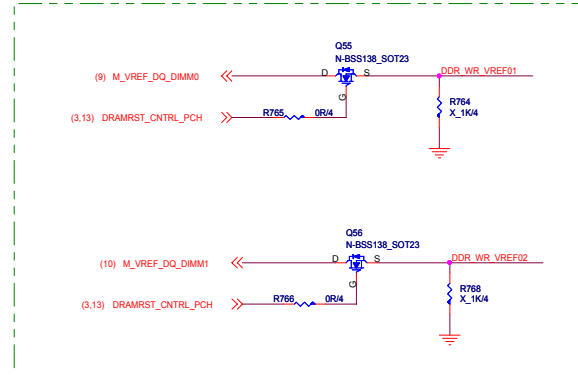
VID[0] Pin C22	VID[1] Pin C24	VCCSA Vout	Required for 2011 processor	Required for 2012 processor
0	0	0.90 V	Yes	Yes
0	1	0.80 V	Yes	Yes
1	0	0.725 V	No	Yes
1	1	0.675 V	No	Yes



IVYBRIDGE PROCESSOR (GND)



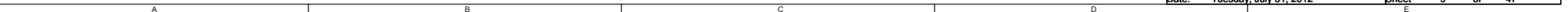
CPU1E			
AK28	CFG[0]	RSVD28	L7
AK29	CFG[1]	RSVD29	AG7
AL26	CFG[2]	RSVD30	AE7
AK27	CFG[3]	RSVD31	AK5
AK26	CFG[4]	RSVD32	W8
AL29	CFG[5]		
AL30	CFG[6]	RSVD33	AT26
AM31	CFG[7]	AM30	AJ27
AM32	CFG[8]	RSVD35	
AM30	CFG[9]		
AM28	CFG[10]		
AM29	CFG[11]		
AN28	CFG[12]		
AN31	CFG[13]	RSVD37	T8
AM29	CFG[14]	H16	
AM27	CFG[15]	RSVD38	H16
AK31	CFG[16]	RSVD39	G16
AK29	CFG[17]	RSVD40	
AJ31	VAXG_VAL Sense	RSVD41	AR36
AH31	VSSAG_VAL Sense	RSVD42	AT34
AJ33	VCC_VAL Sense	RSVD43	AT33
AH33	VSS_VAL Sense	RSVD44	AR35
		RSVD45	
AJ26	RSVD5		
R4	RSVD6		
D1	RSVD7		
F25	RSVD8	RSVD46	B34
F24	RSVD9	RSVD47	A33
F23	RSVD10	RSVD48	A34
D24	RSVD11	RSVD49	B35
B25	RSVD12	RSVD50	C35
B24	RSVD13		
E23	RSVD14		
B23	RSVD15		
C30	RSVD16		
A31	RSVD17		
B30	RSVD18		
B29	RSVD19		
D30	RSVD20		
B31	RSVD21		
A30	RSVD22	RSVD54	AM36
C29	RSVD23	RSVD55	AM35
R20	RSVD24		
B18	RSVD25	RSVD56	AT27
A19	VCCIO_SEL	RSVD57	AT17
		RSVD58	AR17
A15	RSVD27		
		KEY	B1



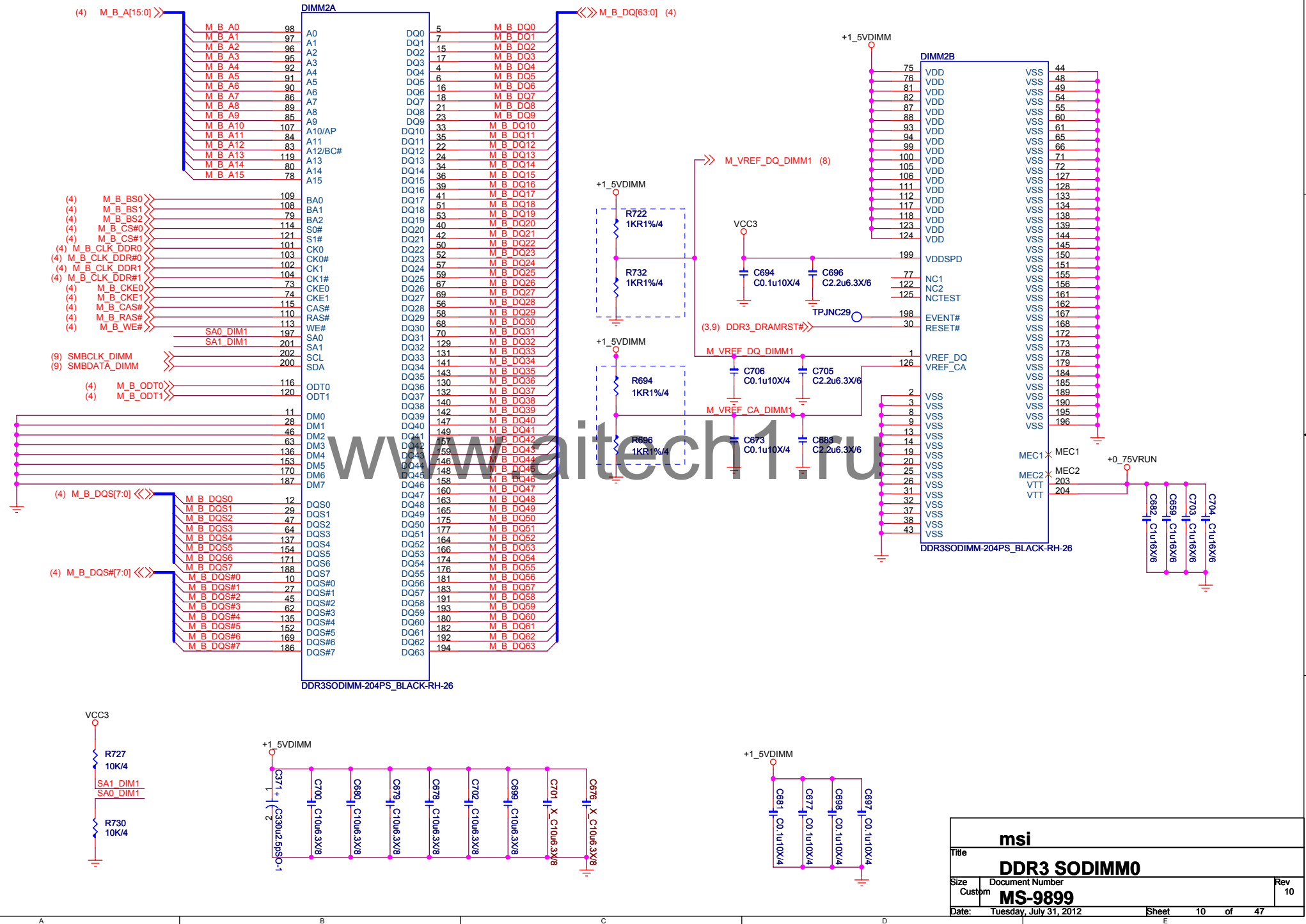
PCI-Express Configuration Select	
CFG[5:6]	<p>11:Default X16-device 1 functions 1 and 2 disabled 10: X8 X8-device 1 functions 1 enable, function2 disabled 01:Reserved--(device 1 functions 1disabled function2 enable 00: X8 X4 X4-device 1 functions 1 and 2 enable</p>

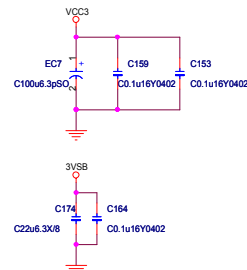
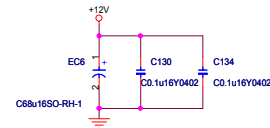
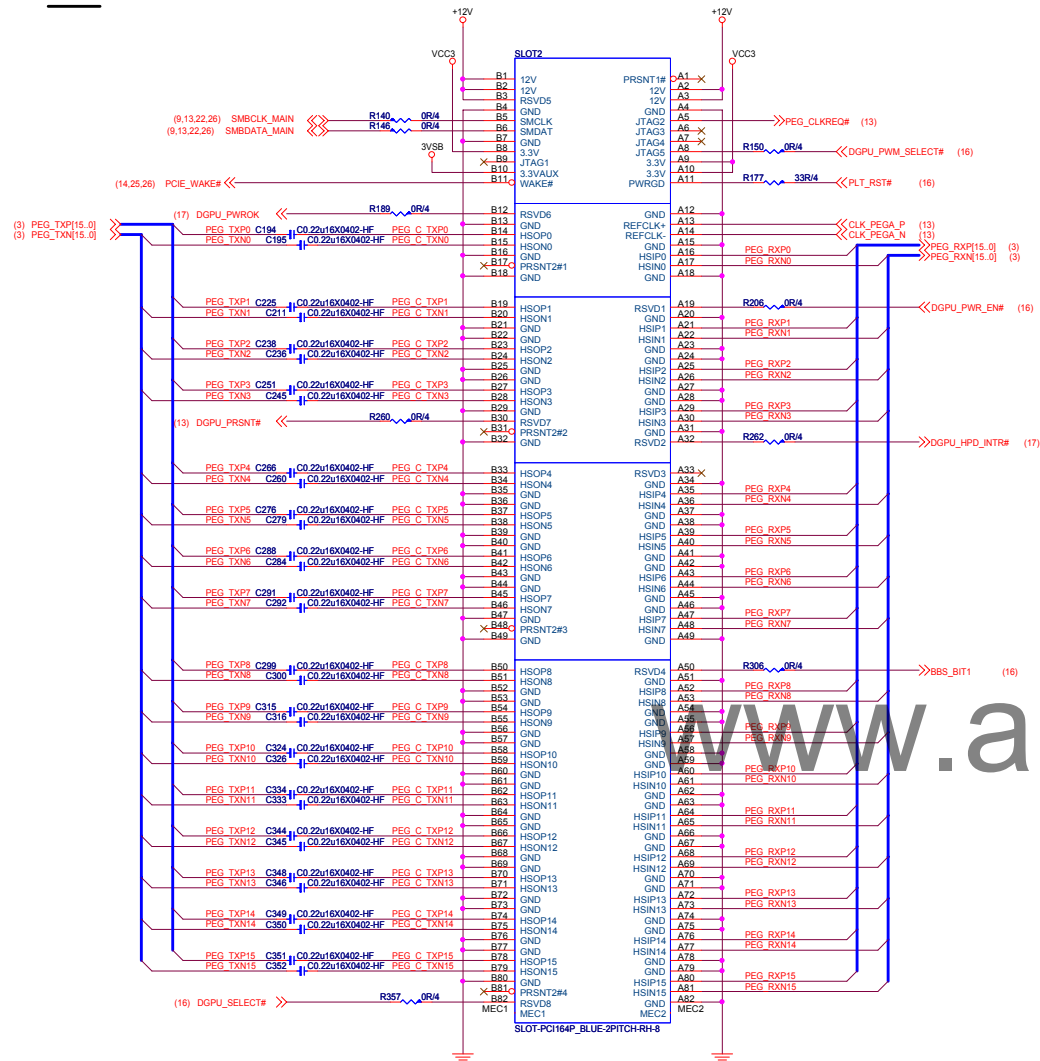
PEG DEFER TRAINING	
CFG7	1 : (Default) PEG train immediately following xxRESETB de assertion 0 : PEG wait for BIOS for training

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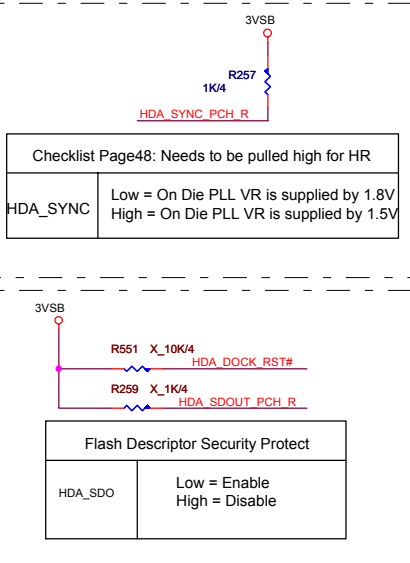
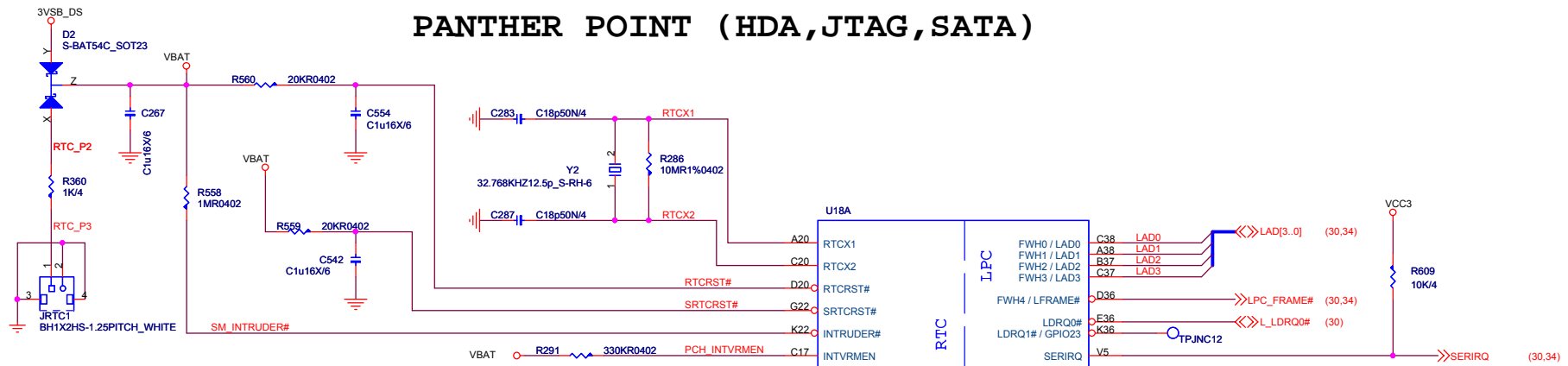


SODIMM#B

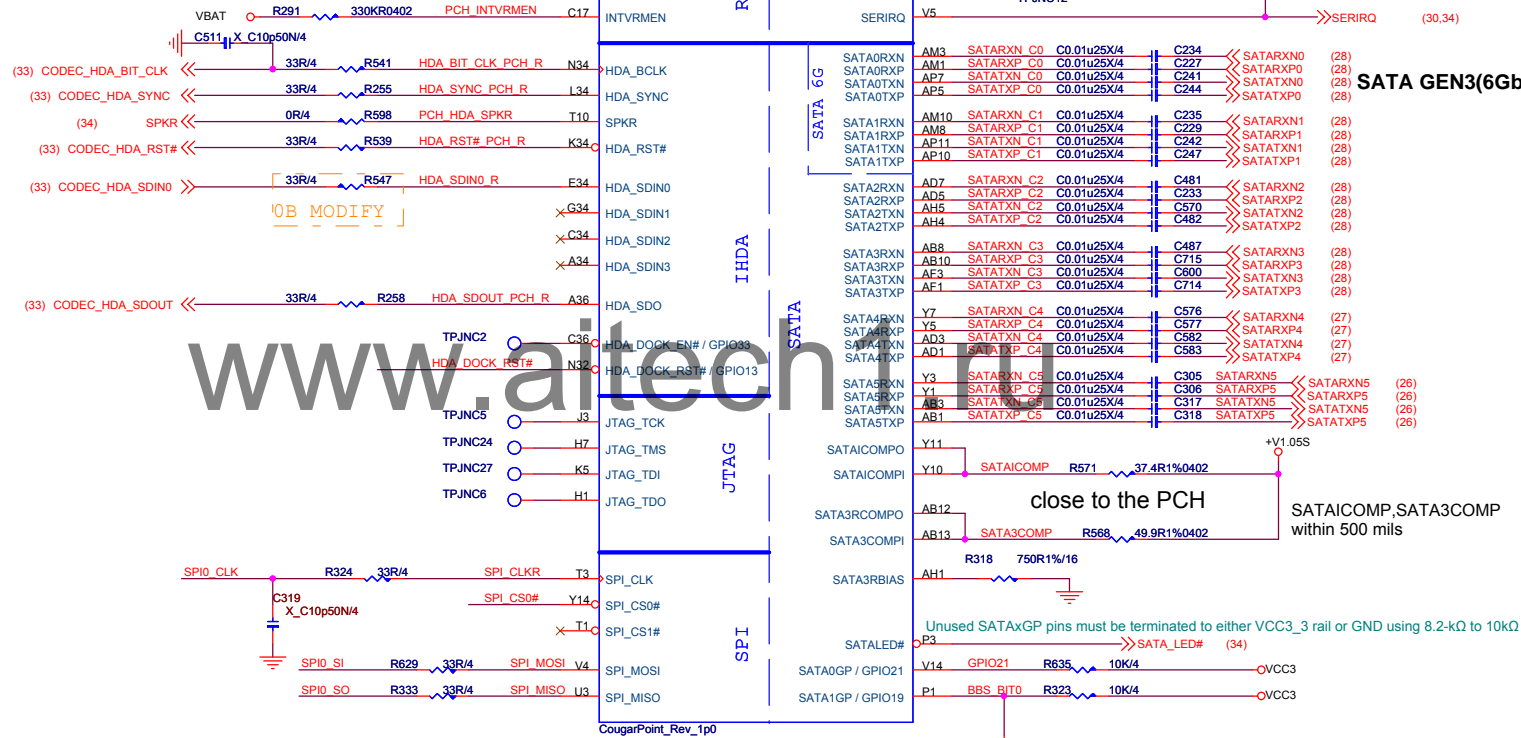
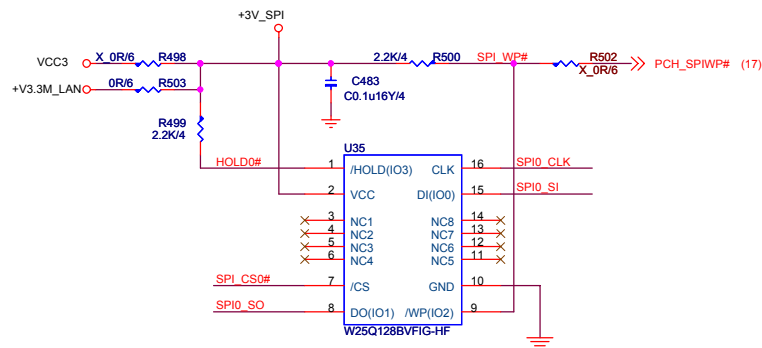




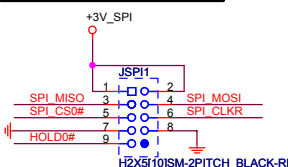
PANTHER POINT (HDA,JTAG,SATA)



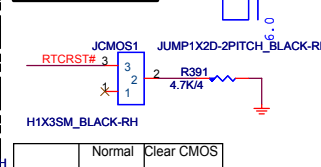
SPI FLASH (128Mb)



SPI Debug Port

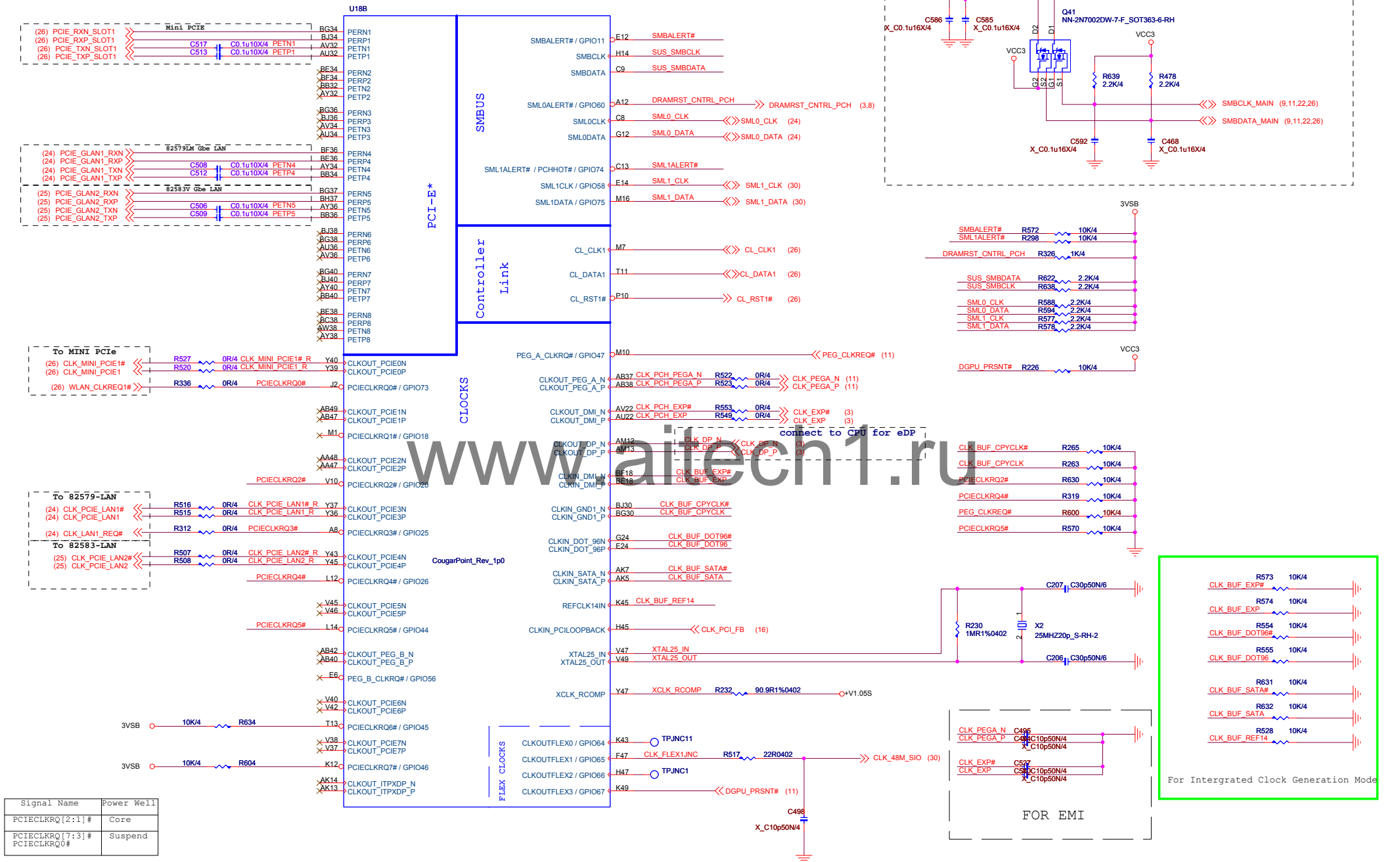


CMOS Jump

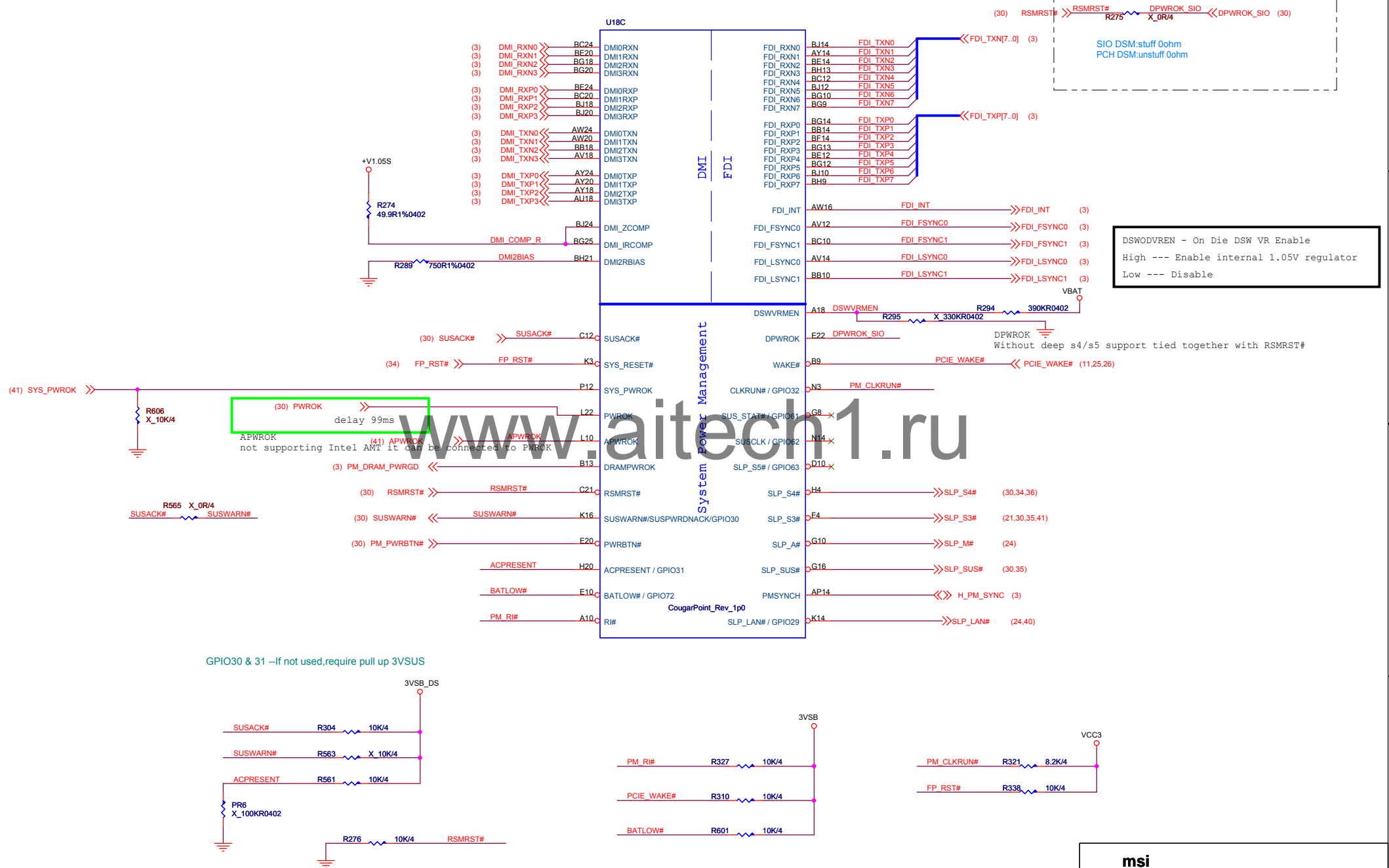


msi		
Title PCH-M (HDA, JTAG, SATA)		
Size	Document Number	Rev
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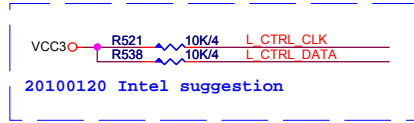
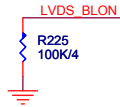
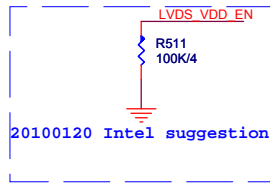
PANTHER POINT (PCI-E, SMBUS, CLK)



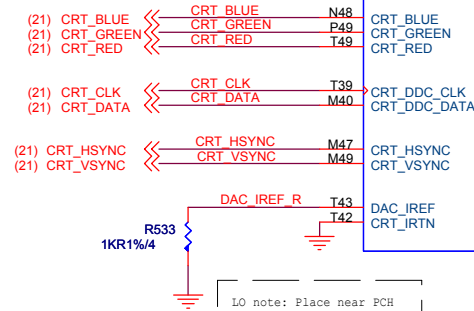
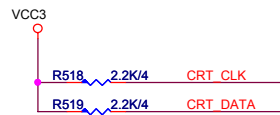
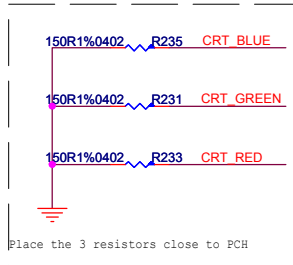
PANTHER POINT (DMI, FDI, GPIO)



PANTHER POINT (LVDS,DDI)



- 1.MXM only LVD_IBG, LVD_VREFH and LVD_VREFL floating. VCCA_LCD and VCCTX_LVD can be connected to GND.
- 2.If use LVDS, LVD_IBG connect 2.37k to GND. LVD_VREFH and LVD_VREFL connect to GND. VCCA_LCD and VCCTX_LVD connect to power.



CougarPoint_Rev_1p0

LVDS

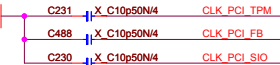
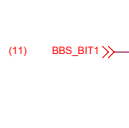
Digital Display Interface

CRT

msi		
Title		
PCH-M (LVDS, DDI)		
Size	Document Number	Rev
B	MS-9899	10
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U18E

Boot BIOS Strap		
BBS_BIT1	BBS_BIT0	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

[illegible]

BRBIAS C33 USB_BIAS R261 22.6R1% 0.0402

SBRBIAS B33

/GPIO5 A14 USB_OCP#0 USB_OCP#0

/GPIO4 K20 USB_OCP#1 USB_OCP#1

/GPIO4 B17 USB_OCP#2 USB_OCP#2

/GPIO4 C16 USB_OCP#3 USB_OCP#3

/GPIO4 L16 USB_OCP#4 USB_OCP#4

/GPIO4 C13 USB_OCP#5 USB_OCP#5

#/GPIO8 D14 USB_OCP#6 USB_OCP#6

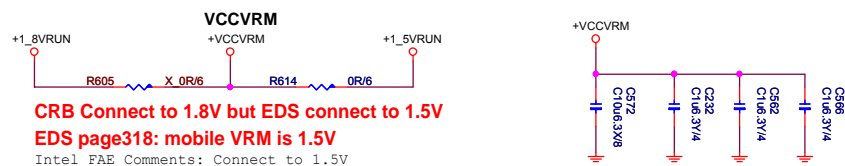
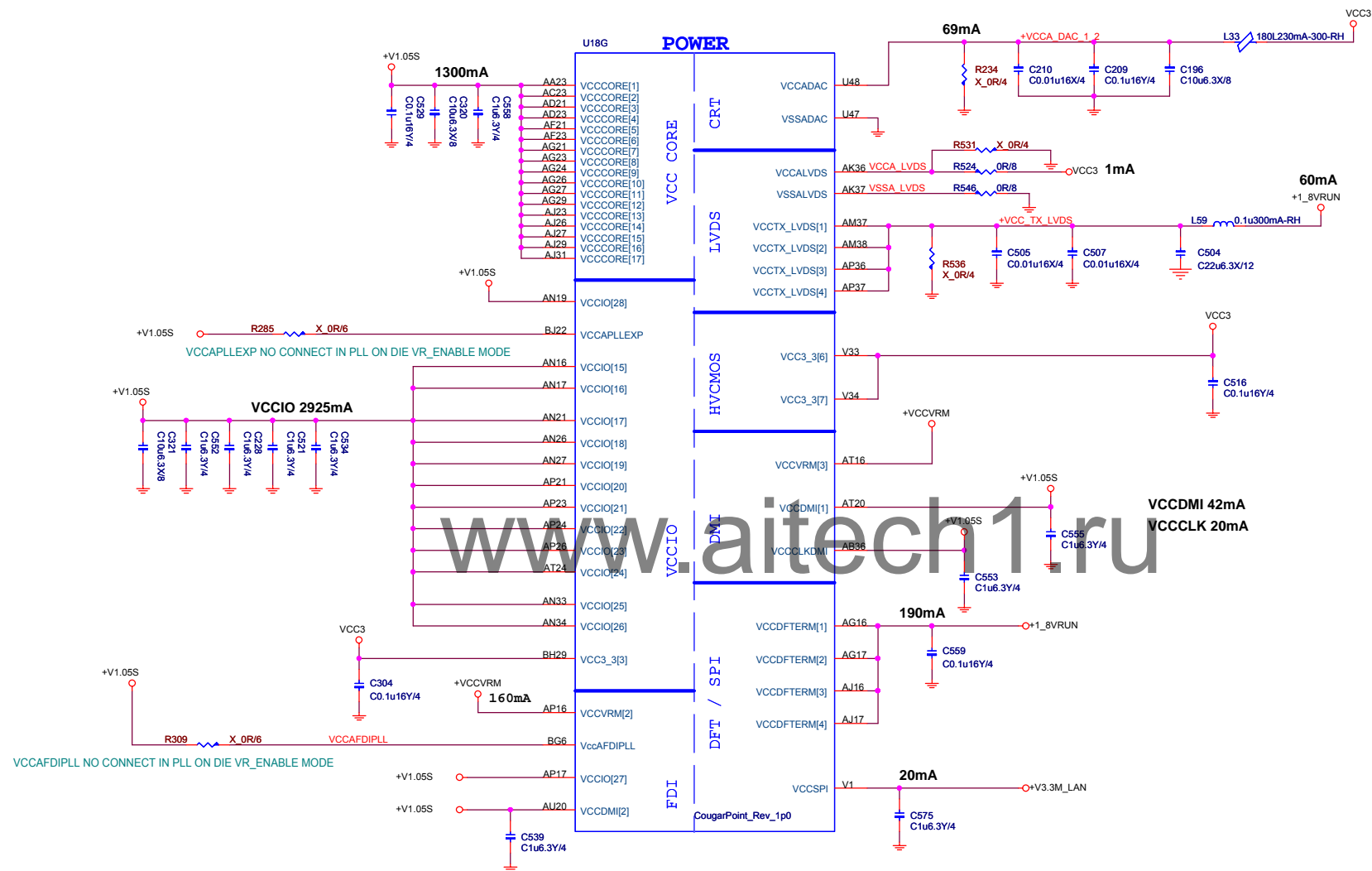
/GPIO10 C14 USB_OCP#7 USB_OCP#7

USB_PN0	USB_PN0	(26)
USB_PP0	USB_PP0	(28)

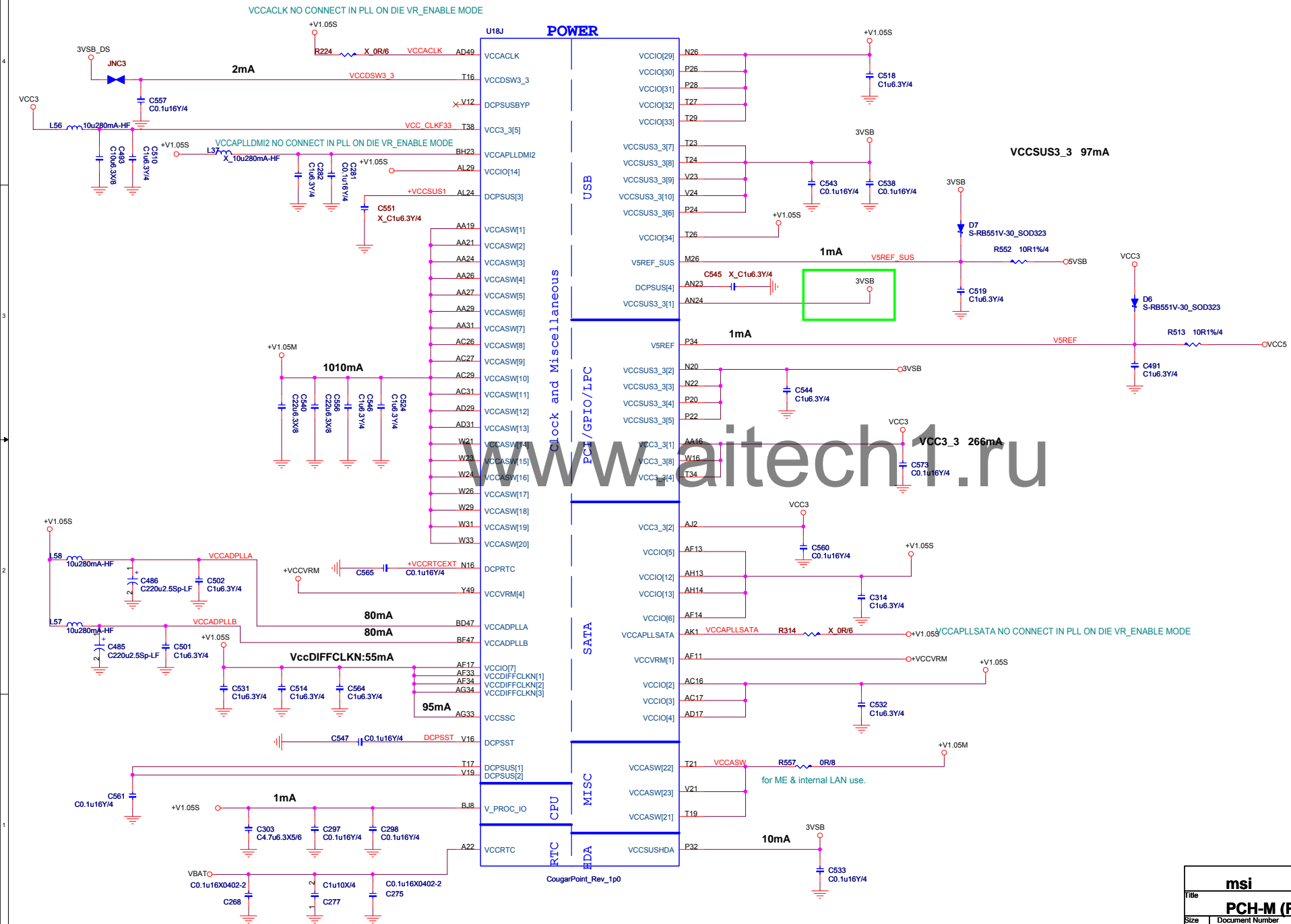
GPIO27 is deep S4 & S5 weak up event,internal pull high.& It's VCCFDIPLL internal VRM strapping pin

msi			
Title			
PCH-M (GPIO, VSS NCTF, RSVD)			
Size	Document Number	Rev	
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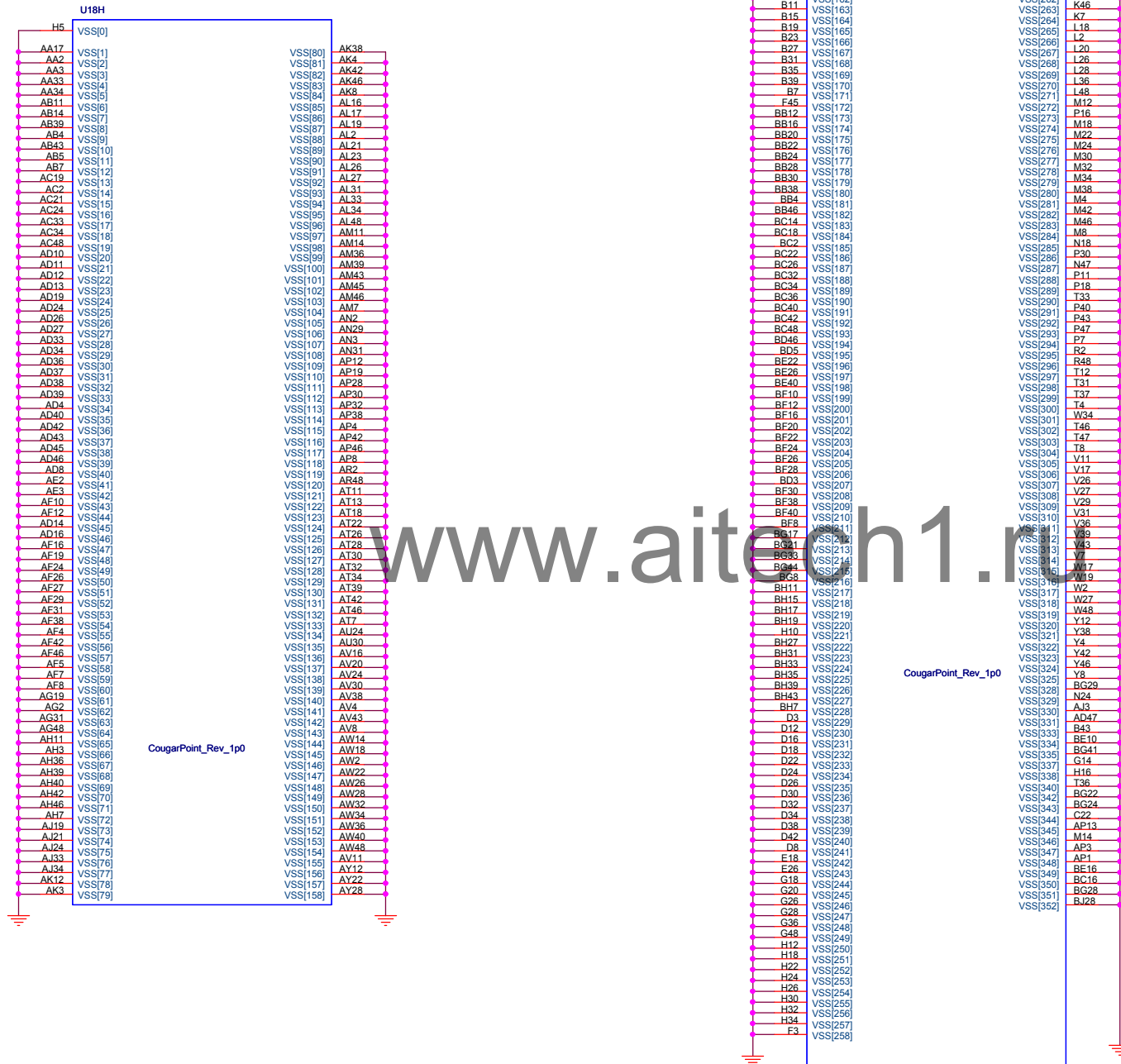
PANTHER POINT (POWER)

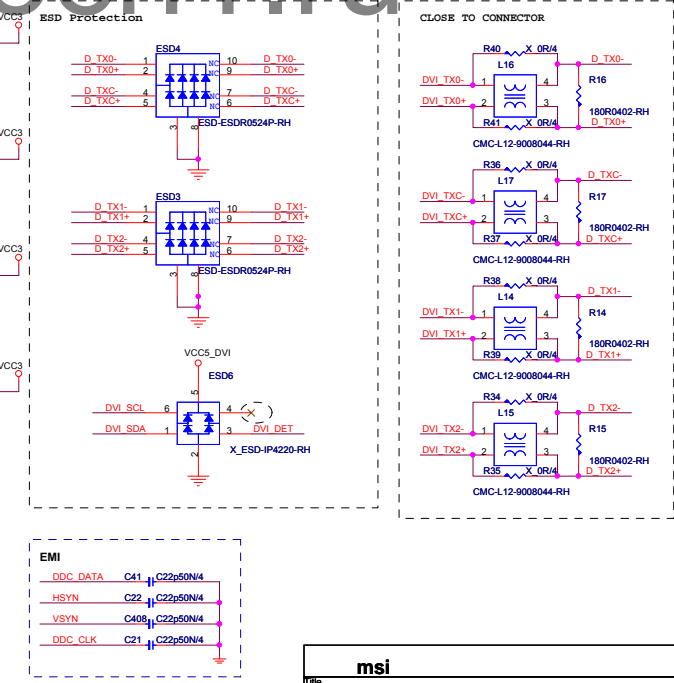
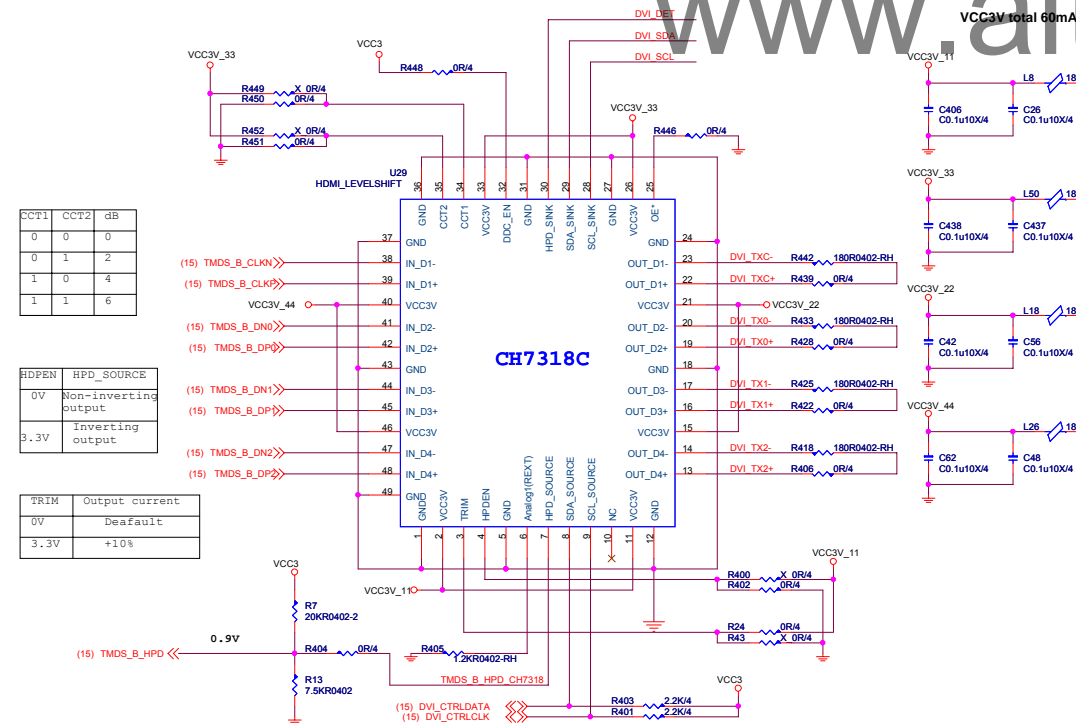
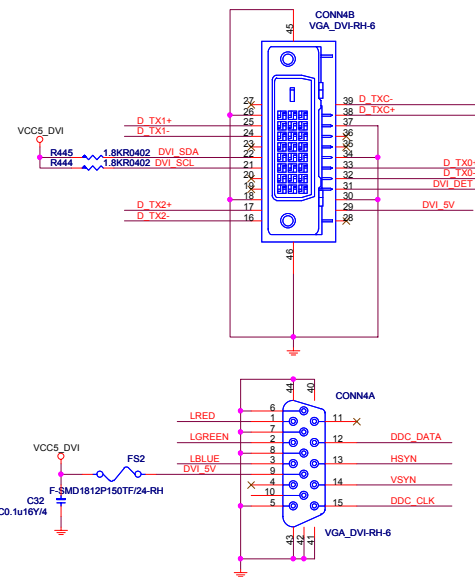
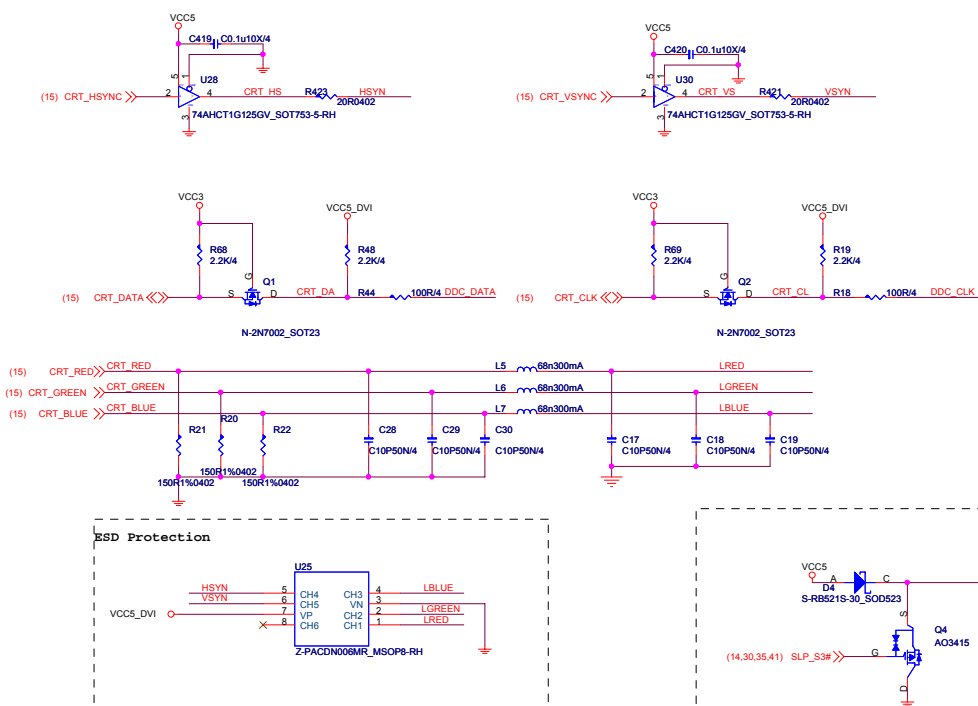


PANTHER POINT (POWER)



PANTHER POINT (GND)





msi

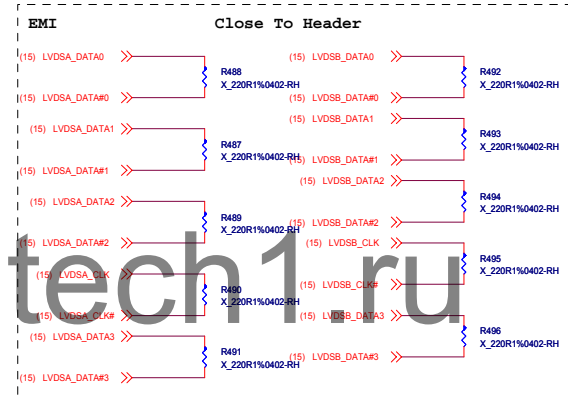
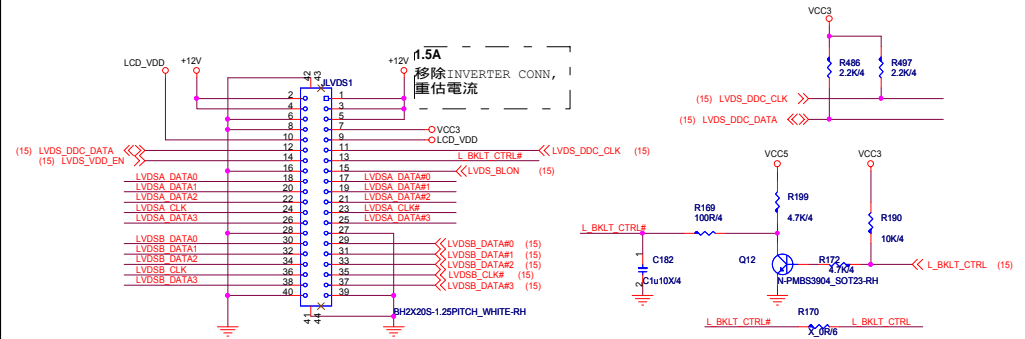
VGA, LVDS, BL

MS-9899

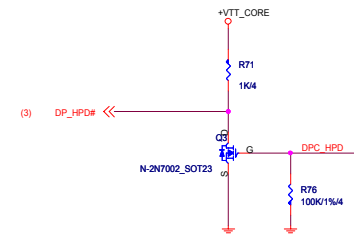
Tuesday, July 31, 2012

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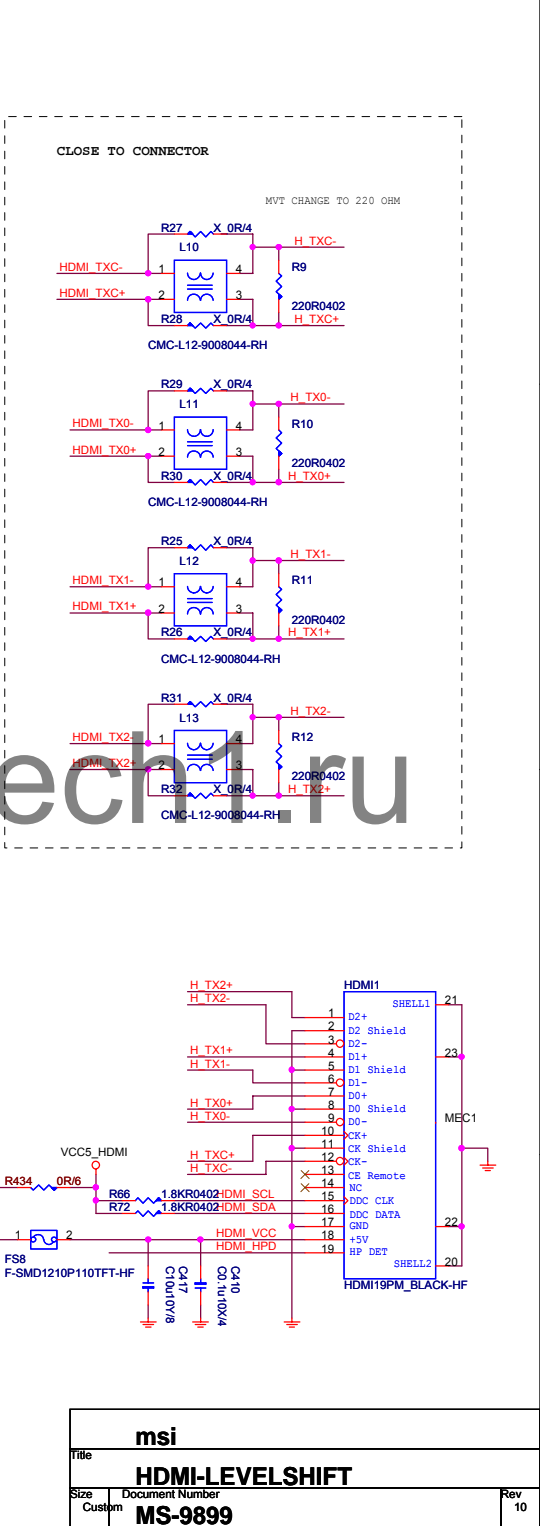
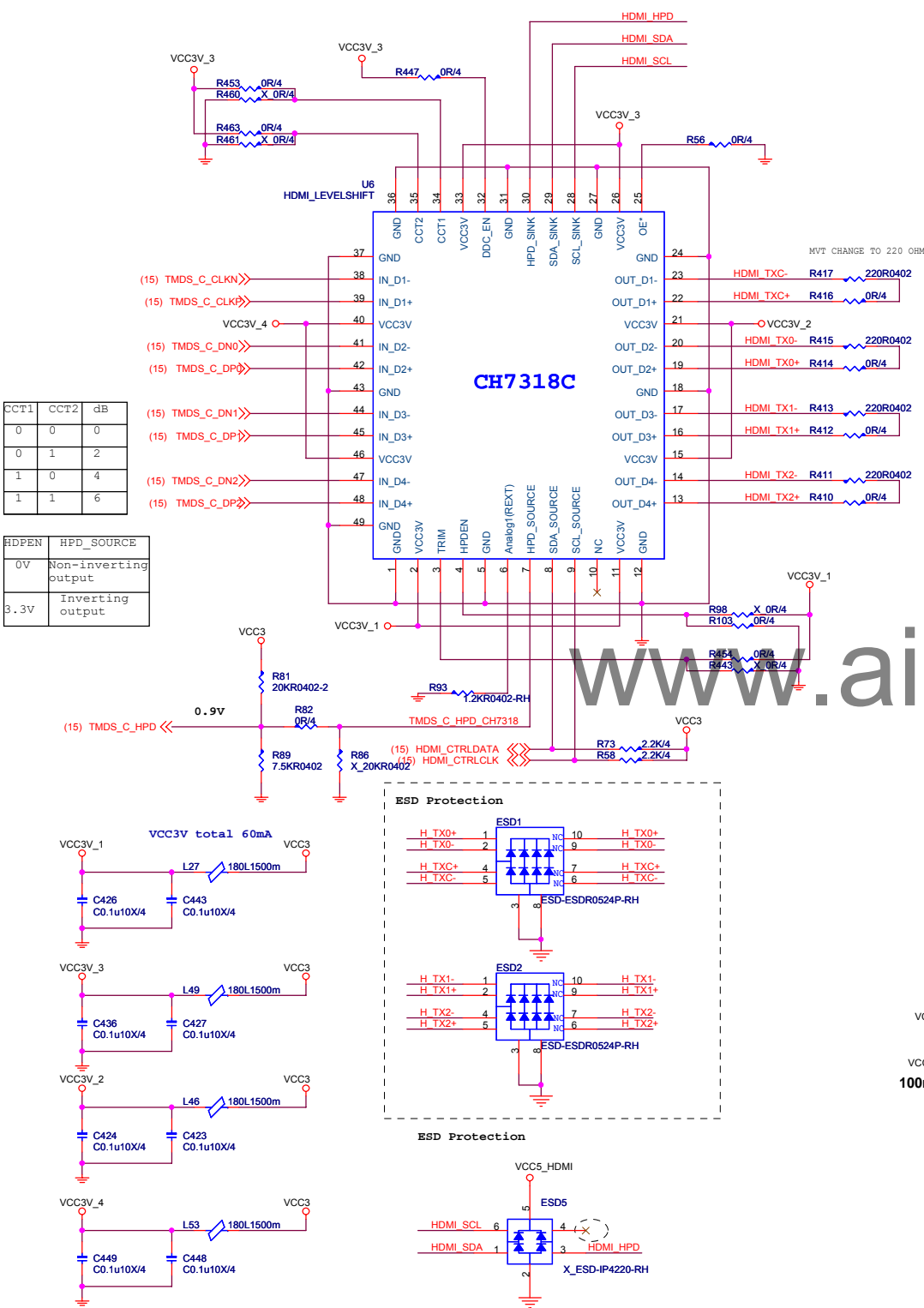
LVDS PIN HEADER

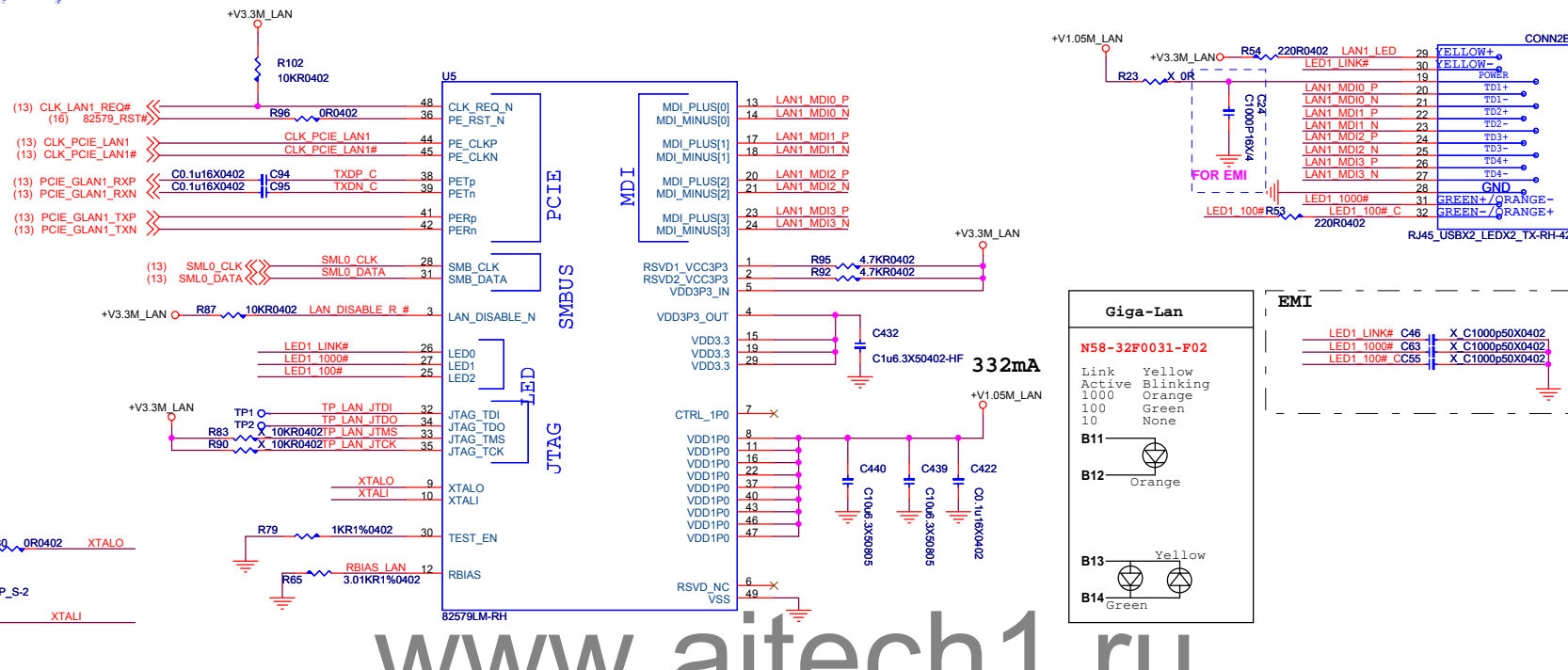


The schematic diagram illustrates the LVDS power supply section. It features a 500mA current source connected to the VCC5 pin of the H1X3M-2PITCH_BLACK-RH-1. The VCC5 pin is also connected to the LCD_SRC pin. The circuit includes a 1.1A-microSMD110-S POLY SWITCH, a 500mA current source, and various capacitors (C158, C167, C191, C226) and resistors (R193, R102, R171, R512). The LVDS_VDD_EN signal is connected to the GND pin of the N-2N7002_SOT23 transistor.

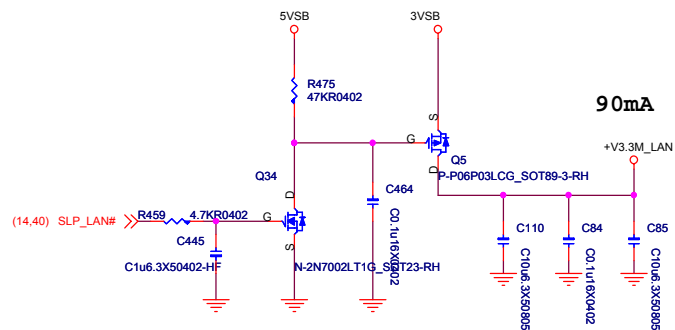


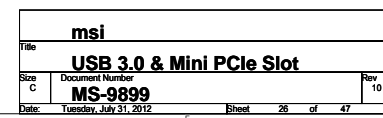
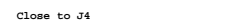
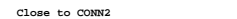
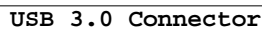
HPD Inversion for eDP



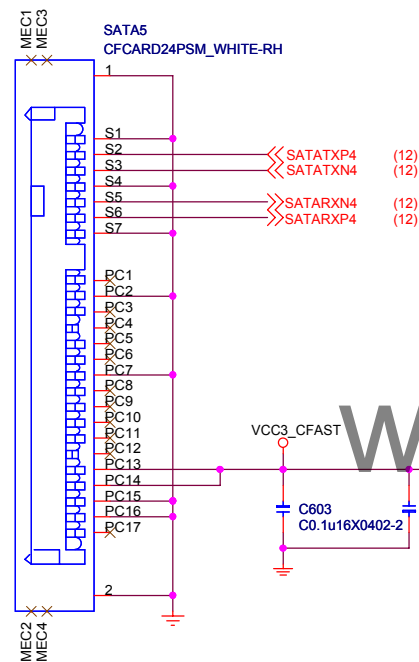
$$V_o = V_{ref} (1 + R_2/R_1) + I_{adj} \times R_2$$
**iAMT 1.05V**

Current :1.01A

[illegible]

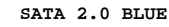
$H = 9\text{mm}$ 

CFast Standard Type



msi			
Title			
CFAST			
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			Rev 10

SATA 3.0 RED



SATA3

(12) SATATXP2
(12) SATATXN2
(12) SATARXN2
(12) SATARXP2

SATA7PM_BLUE-P-RH-1

SATA4

(12) SATATXP3
(12) SATATXN3
(12) SATARXN3
(12) SATARXP3

SATA7PM_BLUE-P-RH-1

DC/PWM MODE

MVT MODIFY FOR FAN SPEED CONTROL

(30) CPU_FANPWM >> R615 10K/4

H : PWM mode
L : DC mode

(30) PWM_FAN_EN >> Q40 2N7002

Q40 2N7002

C0.1u10X/4

C584

U46 TS3211DBVR_SOT23-5-RH

+12V

R612 100R1%/4

+12V D9 S-RB521S-30_SOD523

R627 4.7K/4

R628 100R1%/4

R625 10K/4

CPUFAN1 MEC1

BH1X4B_WHITE-RH-2

Q42 P-SI4435DY-T1-E3_SOIC8-RH

R640 10KR1%/4

R641 3.9KR1%/4042

C720 C10u25X5/206-HF-1

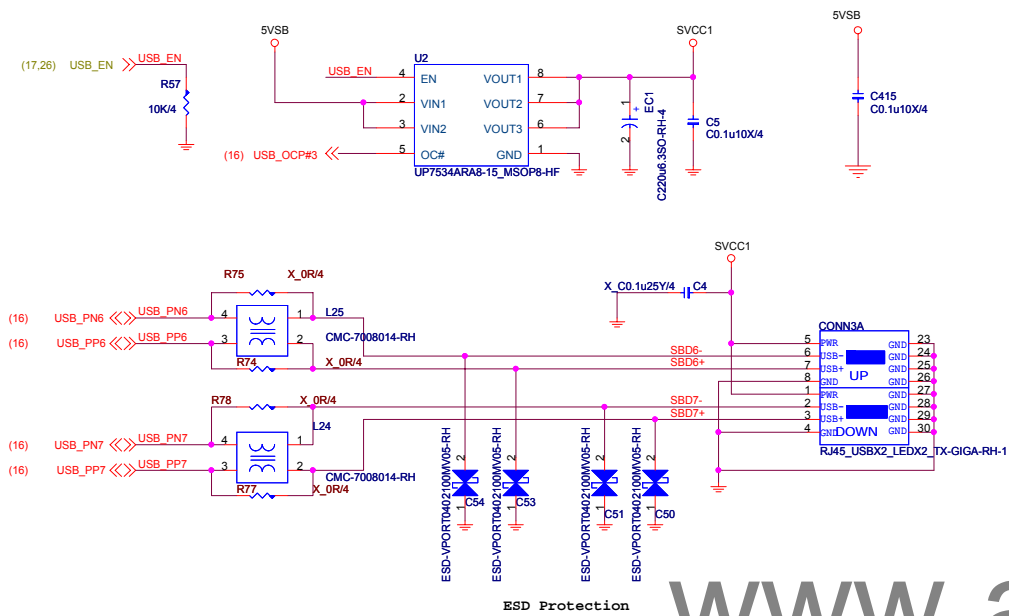
C593 C0.1u10X/4

(30) CPU_FANIN >> R628 100R1%/4

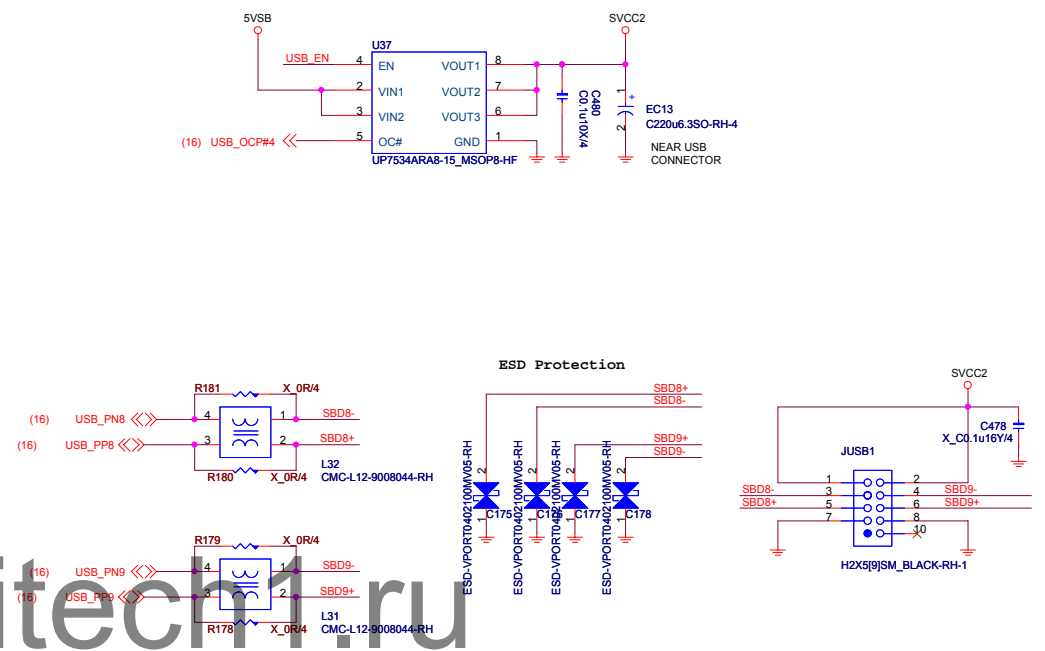
MVT MODIFY FOR FAN SPEED CONTROL

msi			
Title			
SATA, FAN			
Size B	Document Number		Rev
	MS-9899		10
Date:	Tuesday, July 31, 2012	Sheet	28 of 47

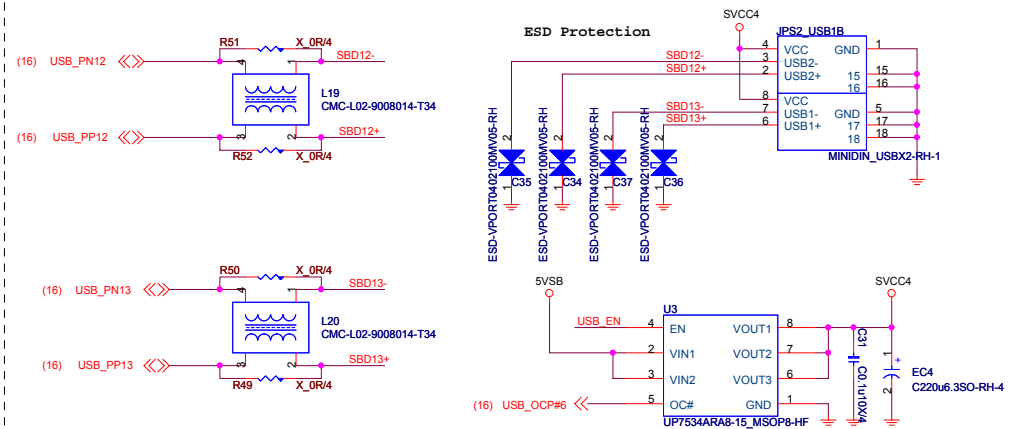
REAR PANEL USB CONNECTOR FOR USB PORT 6,7



INTERNAL PANEL USB CONNECTOR FOR USB PORT 8,9



REAR PANEL USB CONNECTOR FOR USB PORT 12,13

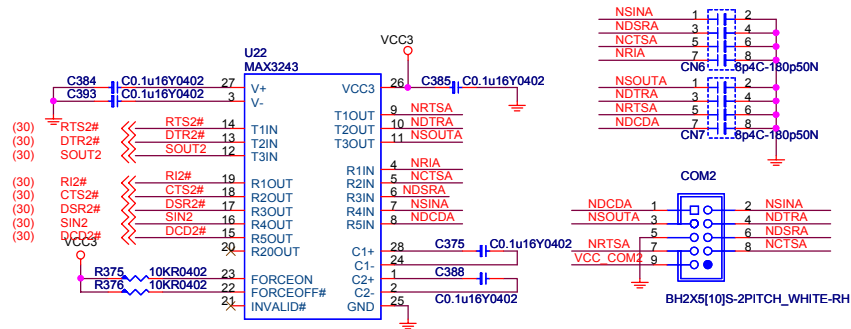


msi			
Title	USB 2.0		
Size	Document Number	Rev	
Custom	MS-9899	10	
Date:	Tuesday, July 31, 2012	Sheet	29 of 47

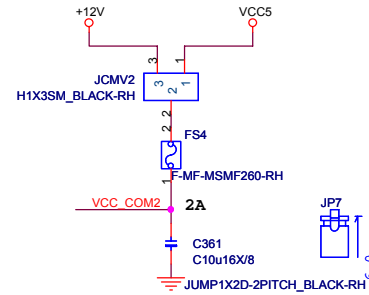


msi			
Title			
SUPER IO (F81866D)			
Size	Document Number		Rev
Custom	MS-9899		10
Date:	Tuesday, July 31, 2012	Sheet	30 of 47

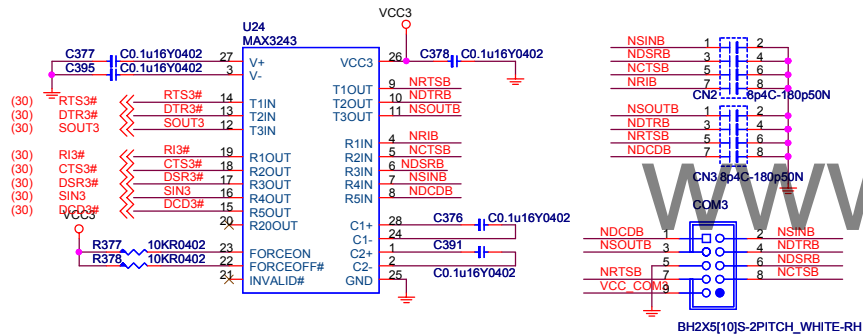
COM PORT 2



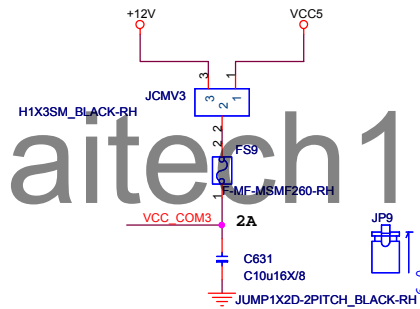
COM2 Voltage Select



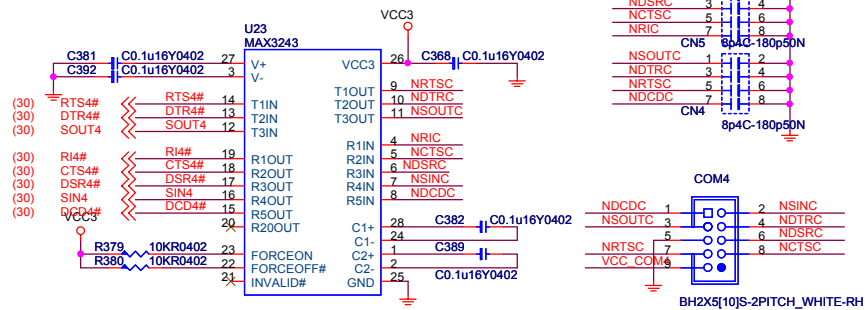
COM PORT 3



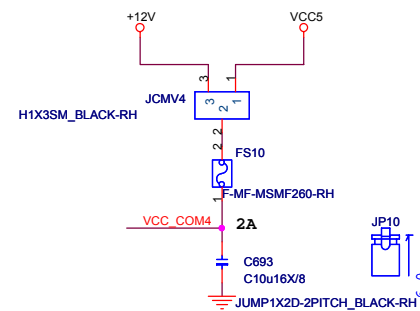
COM3 Voltage Select

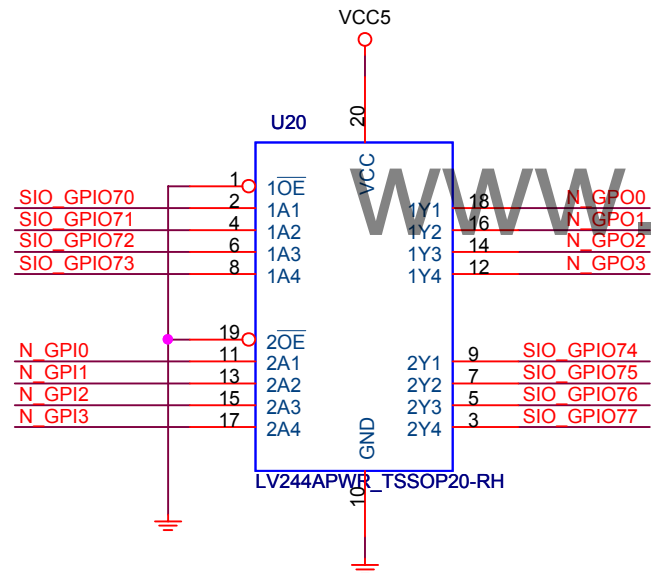
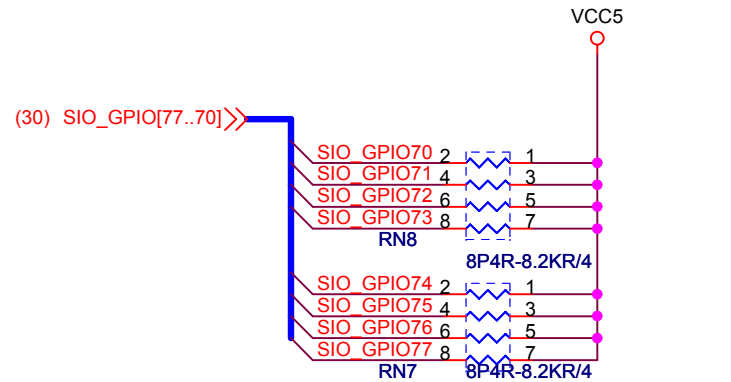


COM PORT 4

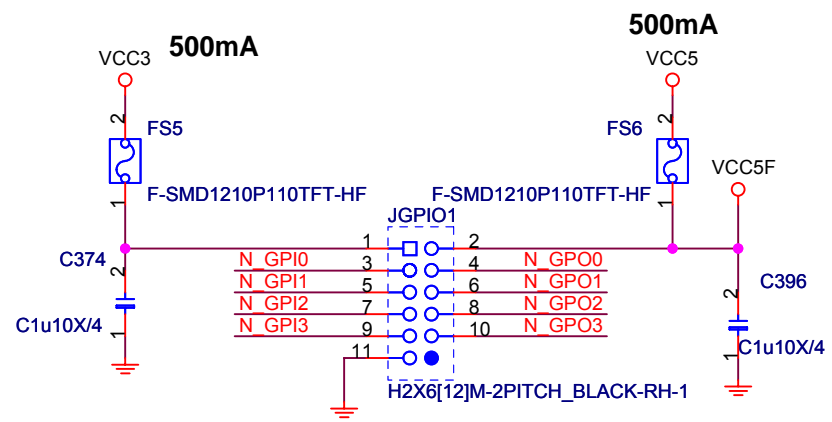


COM4 Voltage Select





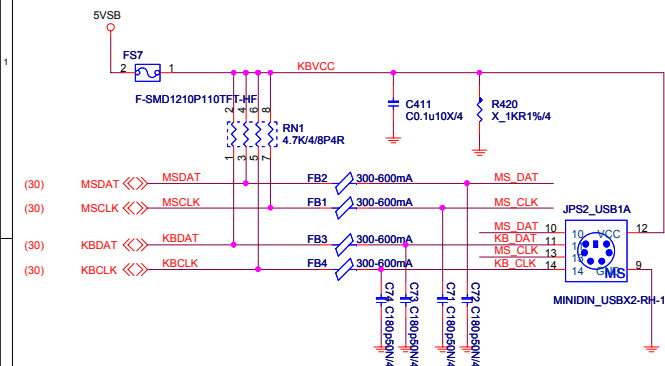
GPIO Pin-header



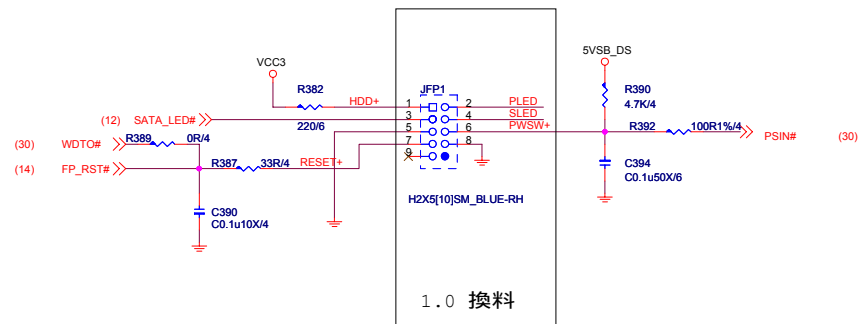
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msi		
Title		
GPIO Conn		
Size	Document Number	Rev
Custom	MS-9899	10
Date:	Tuesday, July 31, 2012	Sheet 32 of 47

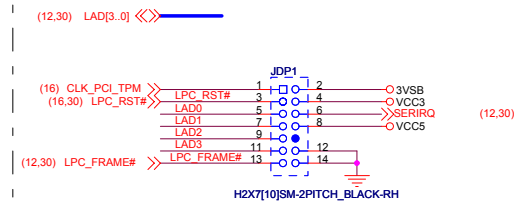
PS2 KEYBOARD & MOUSE CONNECTOR



Front Panel



For SW Debug port 80



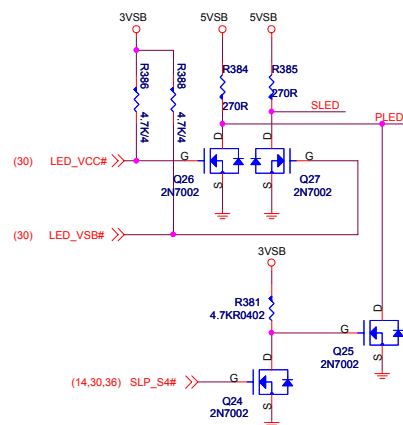
TPM 1.2

TPM_ADDR :
0x02E (Low)
0x04E (High) Default

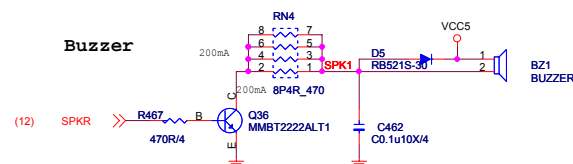
TPM PP: Physical presence standard
connect to GND(floating is GND)

IO Address:0x02E

PWR/Suspend LED



Buzzer



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STATE	LED_VCC#	LED_VSB#	PLED	SLED
S0	0	1	1	0
S3	1-0-1..	1	0-1-0..(1 sec)	0
S5	1	1	0	0

msi			
Title			
FRONT PANEL,PS/2,TPM			
Size	Document Number	Rev	
Custom	MS-9899	10	
Date:	Tuesday, July 31, 2012	Sheet	34 of 47

The schematic diagram illustrates the power supply section of the PWRCONN1 connector. The connector pins are numbered 1 through 24. The power rails and their connections are as follows:

- VCC3:** Connected to pins 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24.
- VCC5:** Connected to pins 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24.
- VCCB_DS:** Connected to pins 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24.
- +12V:** Connected to pins 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24.
- Ground:** Connected to pins 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24.

Key components and their connections include:

- Capacitors:** C99, C295, C289, C259, C285, C152, C479, and C100 are connected to various power rails and ground.
- MOSFET:** Q44 (N-2N7002_SOT23) is connected to the ATX_PSON# signal and the SLP_S3# signal.
- Signals:** ATX_PSON# and SLP_S3# are connected to the connector pins.

[illegible][illegible]

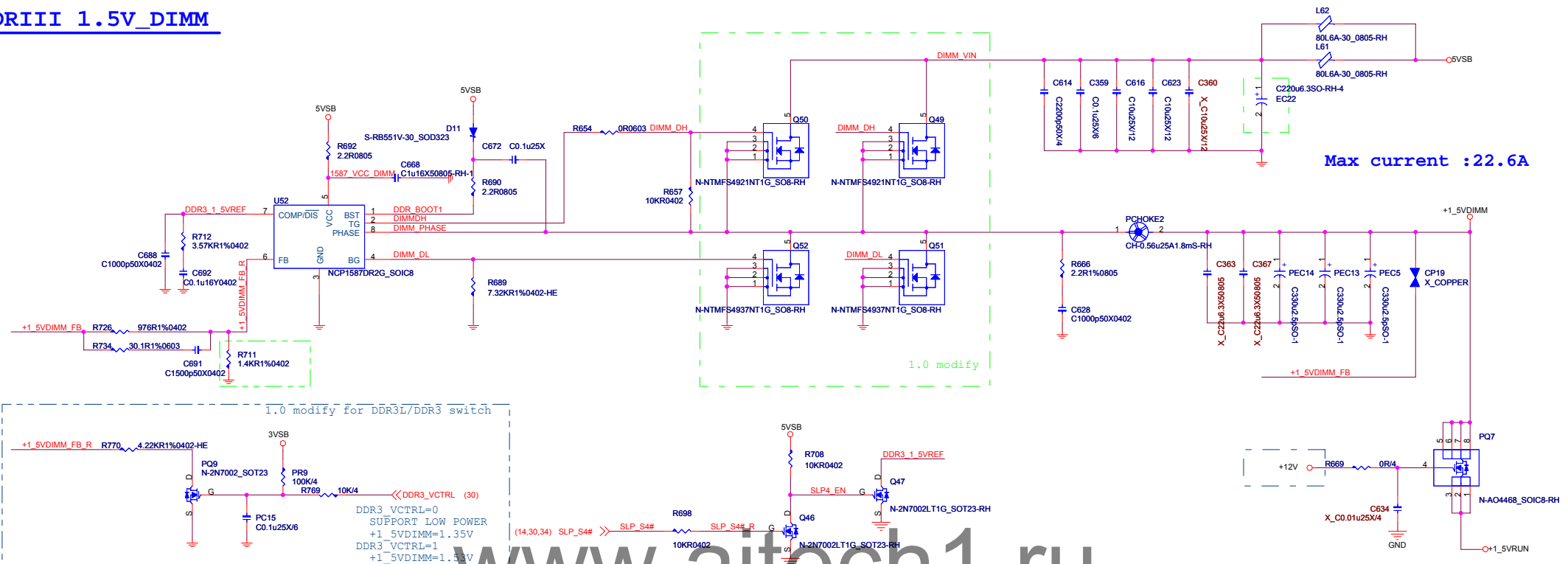
S5#	S3#	MODE	5VDUAL	REMARKS
1	1	X	5VCC	S0/S1/S2 (ACTIVE)
1	0	X	5VSB	S3
0	X	1	5VSB	S4/S5
0	X	0	SHUTDOWN	S4/S5

Title	ATX & DSW POWER
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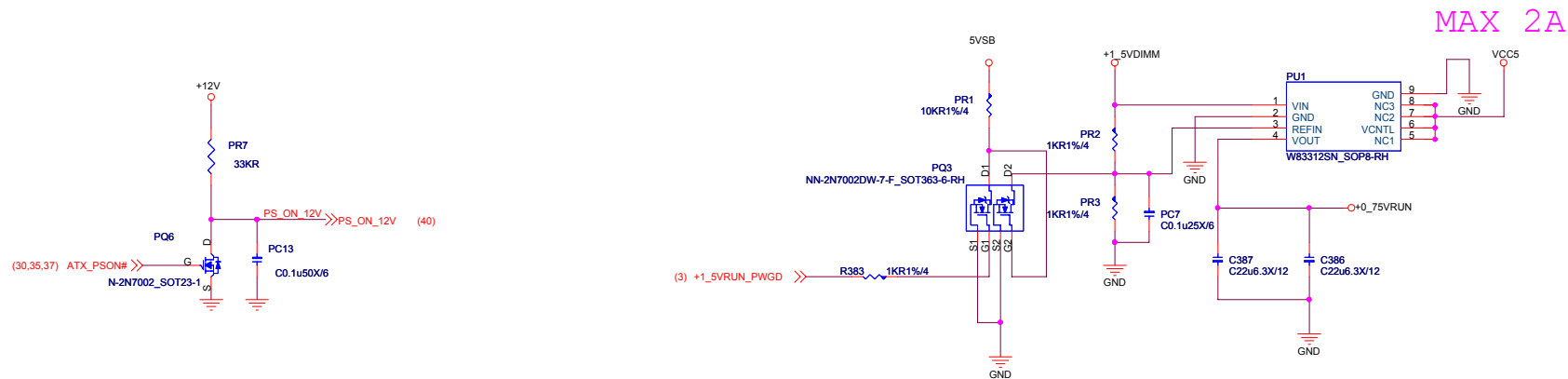
Rev
10

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DDRIII 1.5V_DIMM

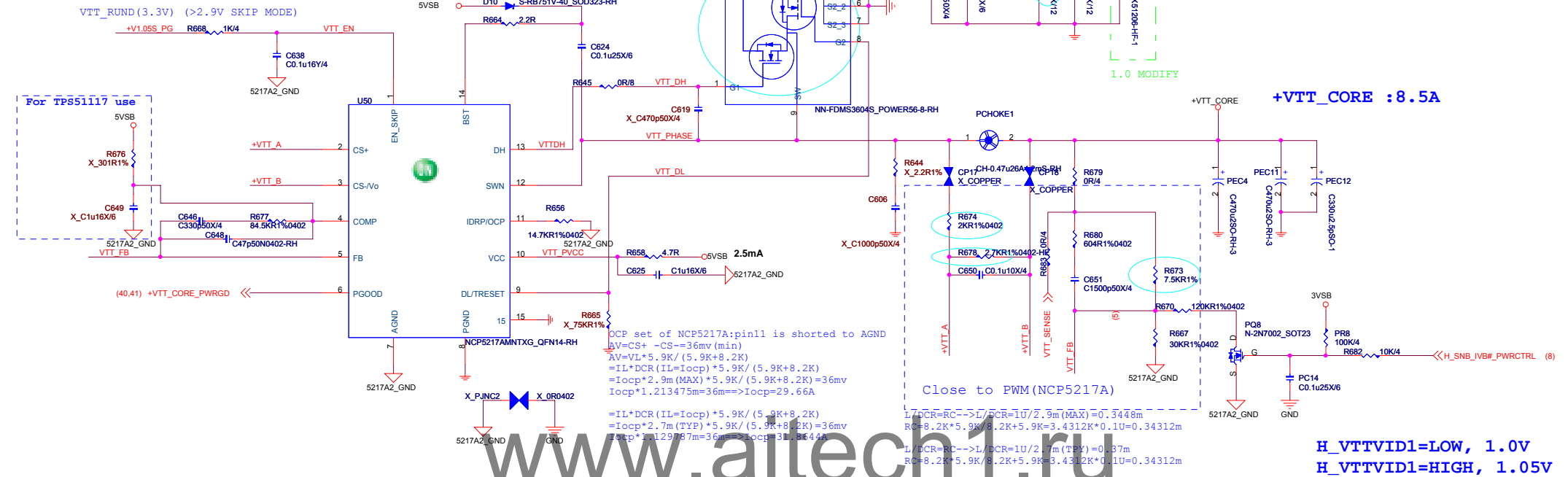


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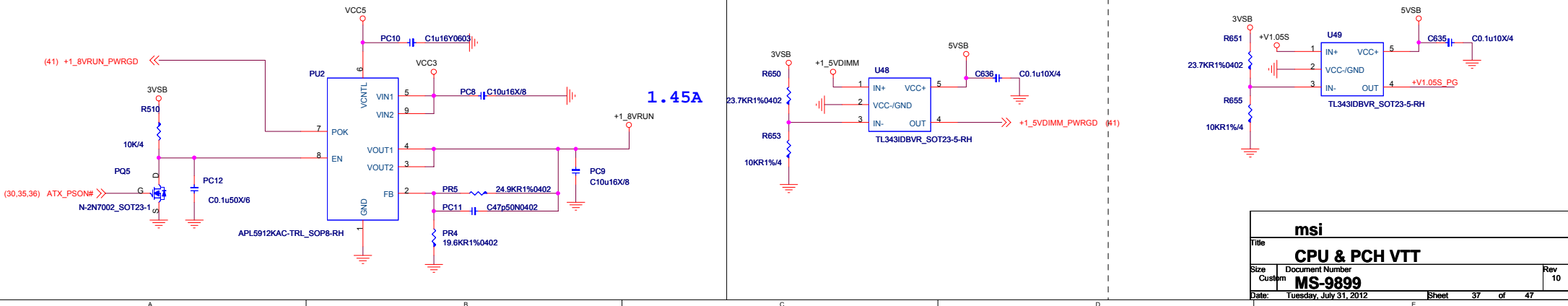


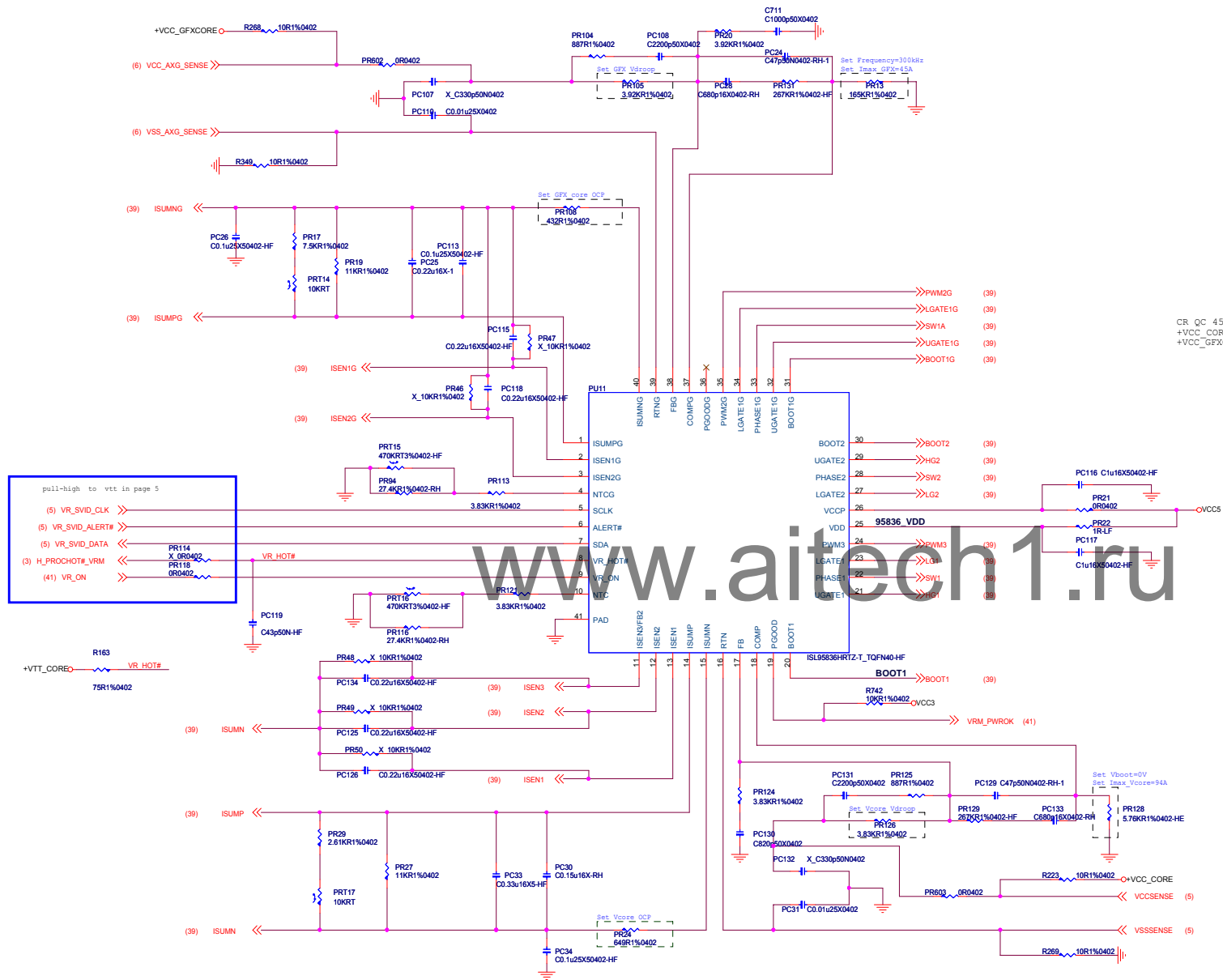
msi			
Title			
DDRIII 1.5V_DIMM			
Size	Document Number	Rev	
Custom	MS-9899	10	
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CPU_VTT



1.8V

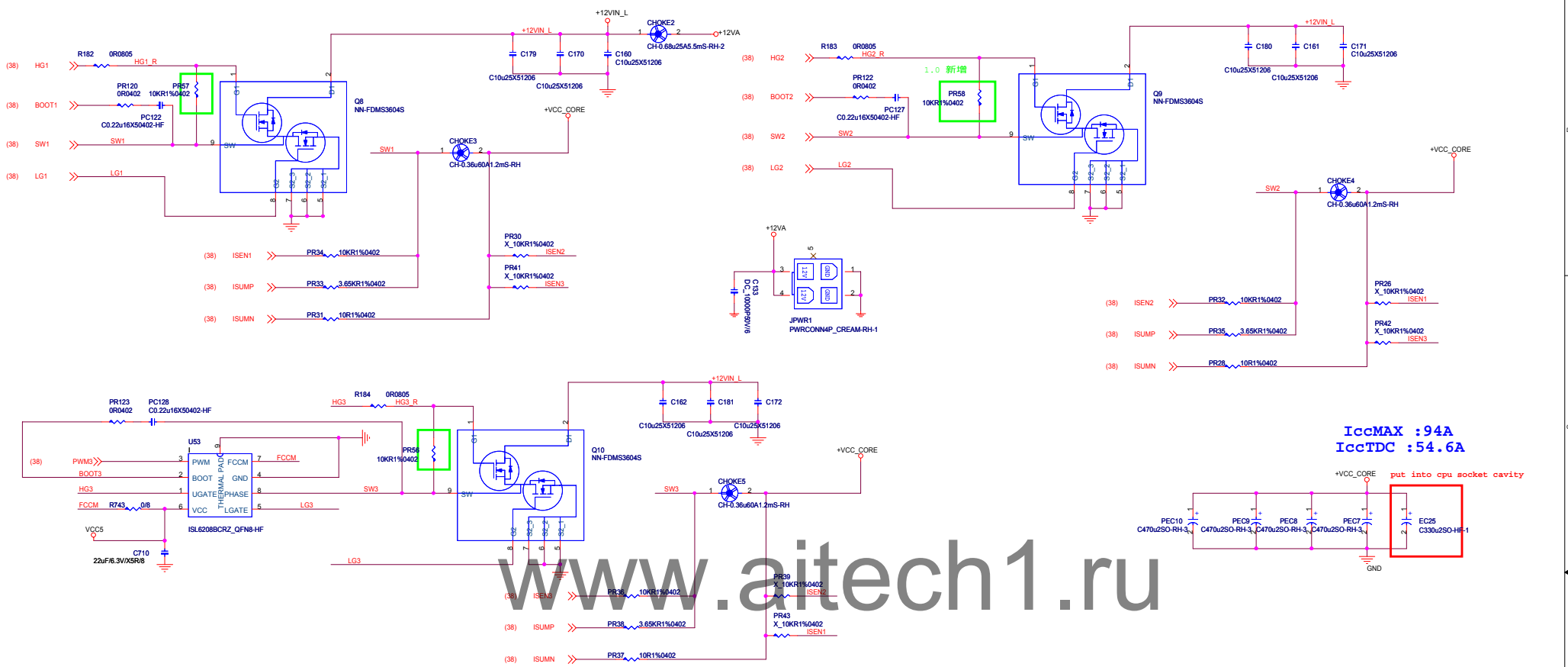




CR QC 45W
 +VCC_CORE ICCMAX=94A R_LL=-1.9mV/A
 +VCC_GFXCORE ICCMAX=46A R_LL=-3.9mV/A

1.0 更改Solution

msi		
File	IMPV7 ISL95835HR	
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C	MS-9899	10
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IccMAX : 94A
IccTDC : 54.6A

put into cpu socket cavity

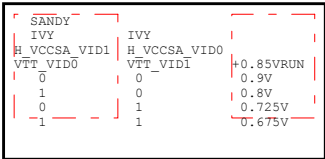
IccMAX : 46A
IccTDC : 35A

put into cpu socket cavity

1.0 更換Solution

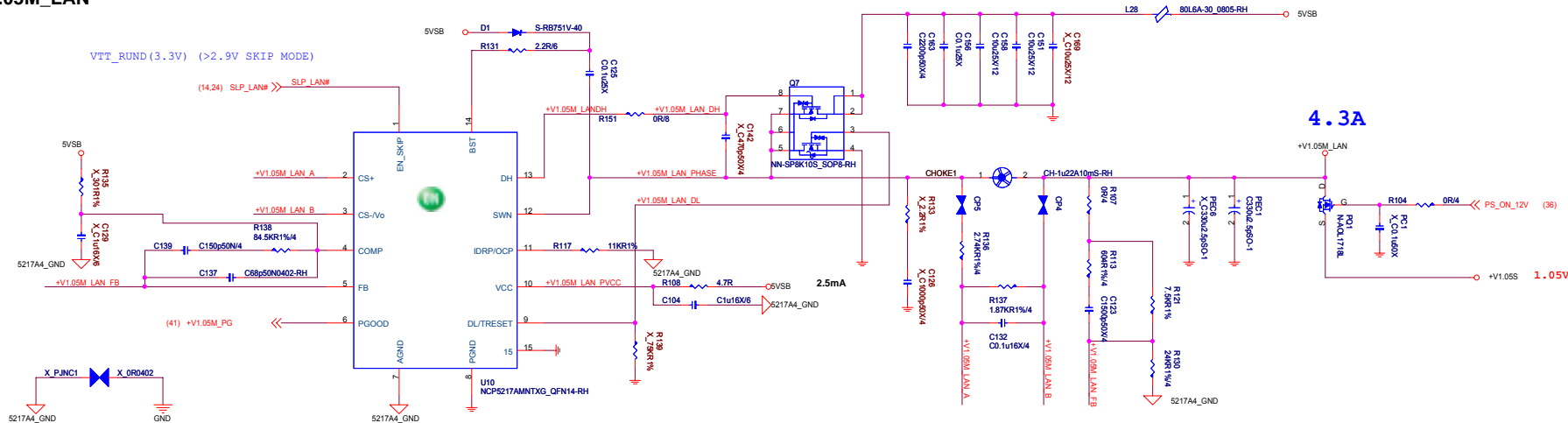
msi			
File	IMVP7 Driver ISL6208		
Size	Document Number	Rev	
C	MS-9899	10	
Date:	Tuesday, July 31, 2012	Sheet	39 of 47

HOLD OFF CPU_SA UNTIL +CPU_VTT IS VALID

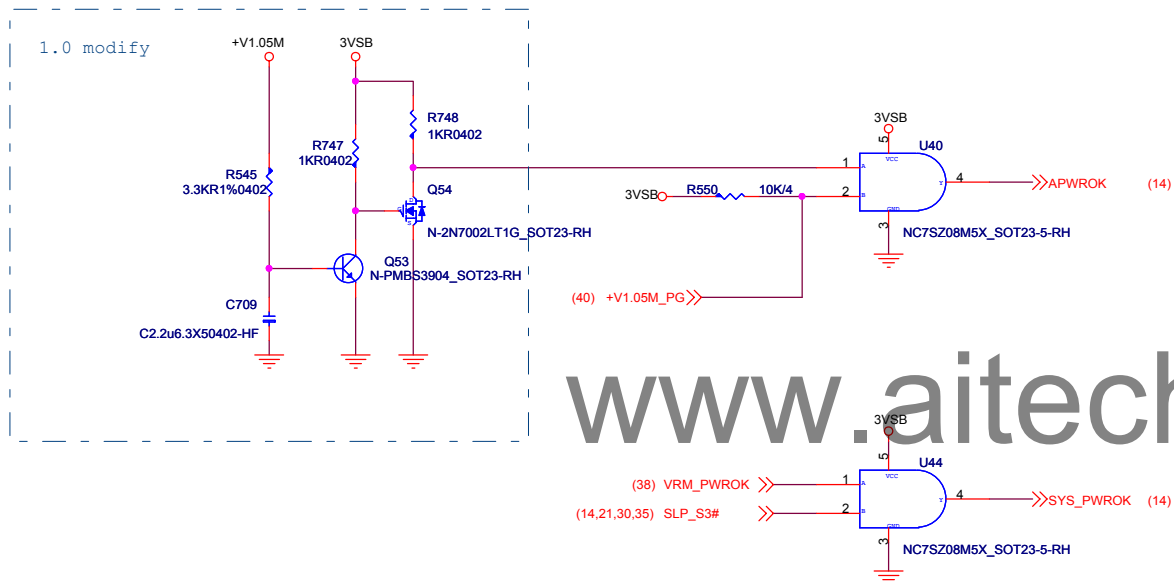
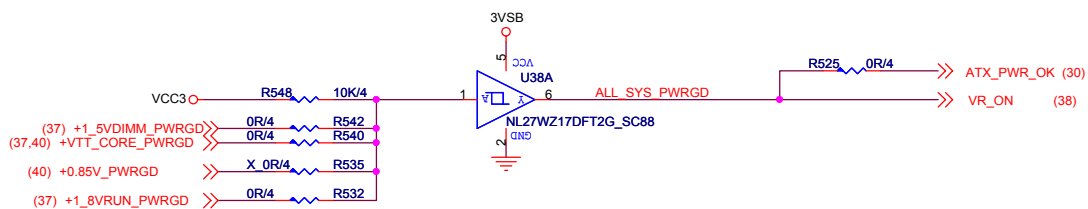


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VTT_RUND (3.3V) (>2.9V SKIP MODE)

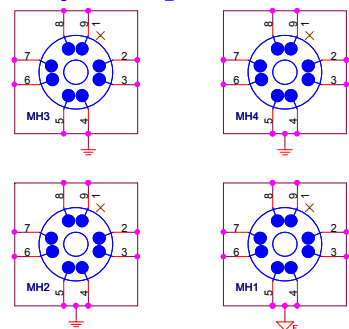


Power Sequence Control

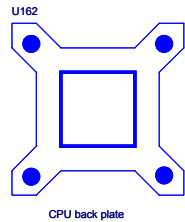


Mounting Holes

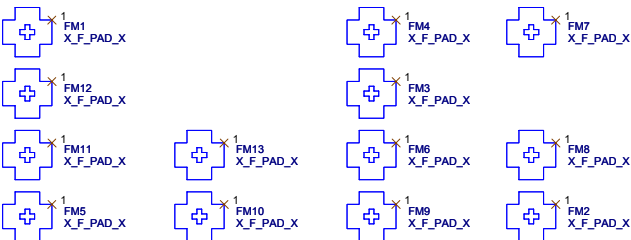
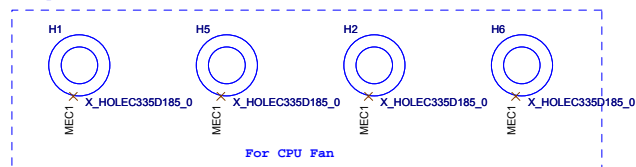
Footprint: HOLES_4S



CPU Back Plate

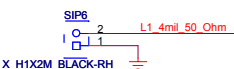


Footprint: H_NR240D140

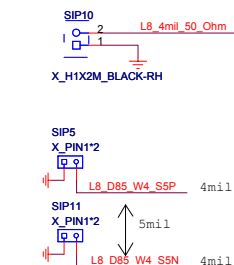


Simulation

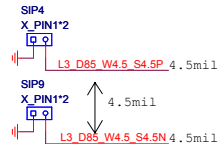
TOP Layer



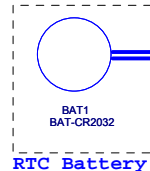
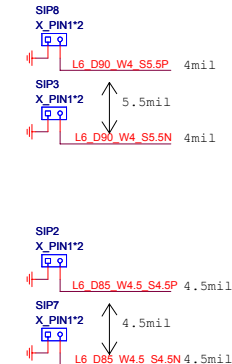
Bottom Layer



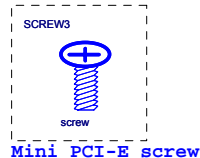
INT3 Layer



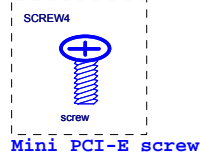
INT6 Layer



RTC Battery

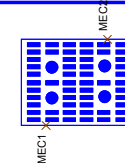


Mini PCI-E screw



Mini PCI-E screw

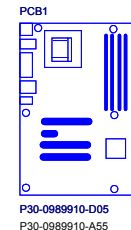
PCH HEAT-SINK



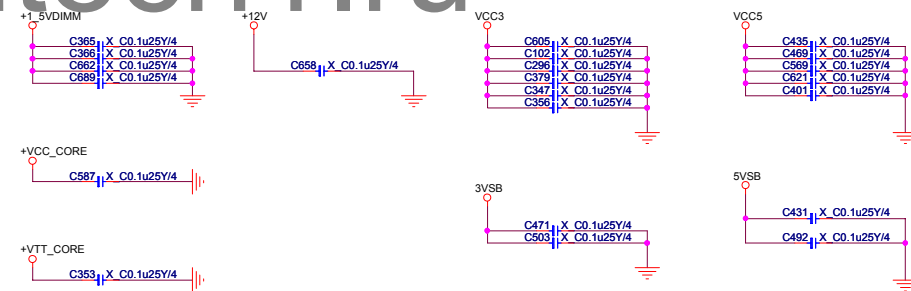
U28_H1
HS-0401470



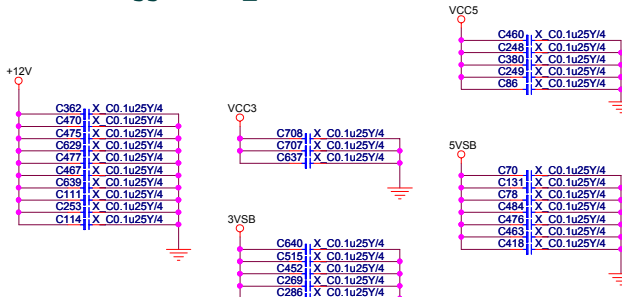
PCB



For EMI Suggestion

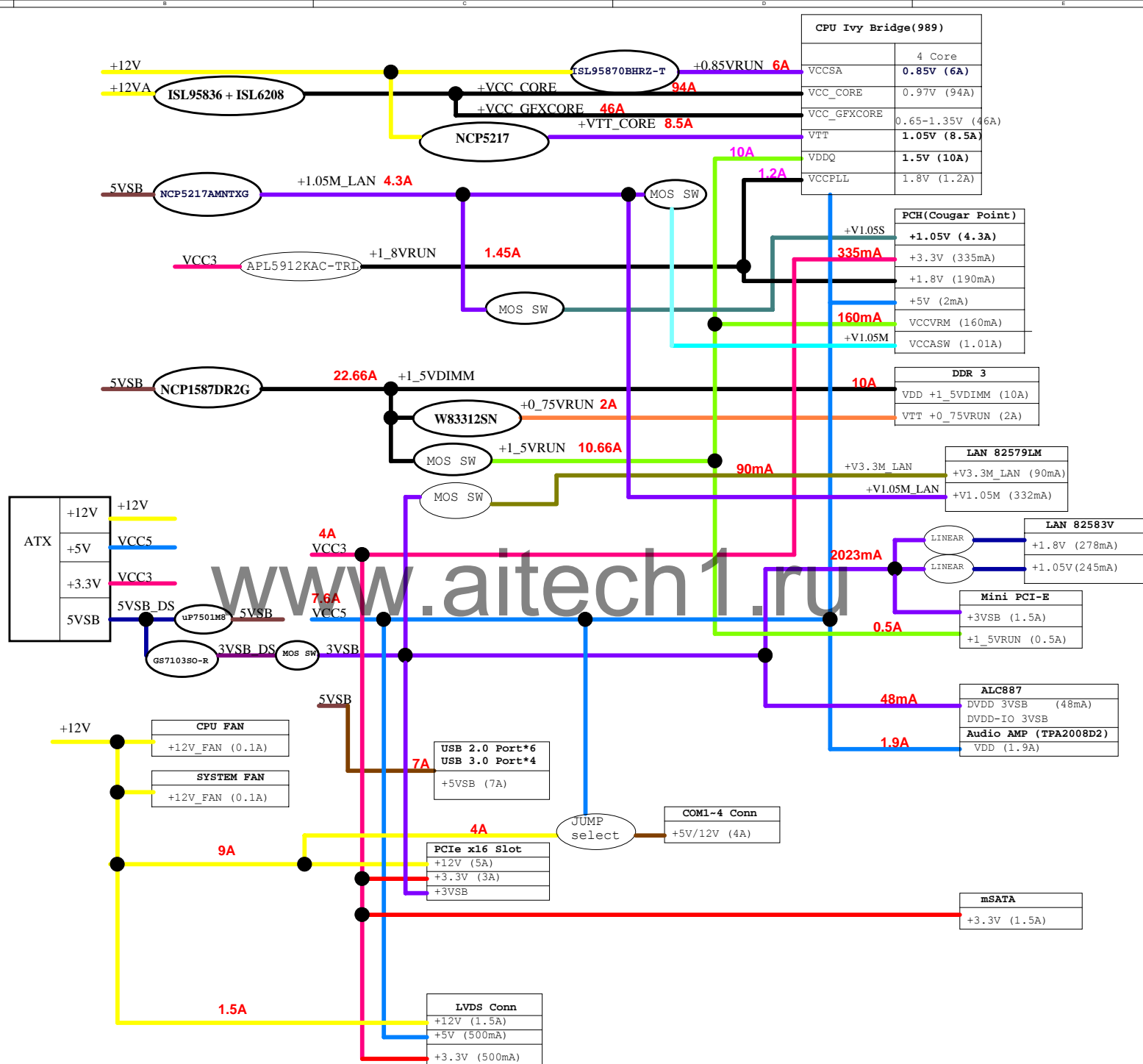


For EMI Suggestion_12/28



msi		
Title	Screw / EMI / BOM-Option Parts	
Size	Document Number	Rev 10
Customer	MS-9899	
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VCC_CORE = 94A
+V1.05M_LAN = 4.3A
+VCC_GFXCORE = 46A
+1_8VRUN = 1.45A
+1_5VDIMM = 22.66A
+0_75VRUN = 2A
+1.5VRUN = 10.66A
3VSB_DS = 2.17A
5VSB_DS = 9.5A
VCC5 = 7.6A
VCC3 = 4A



PCH: Panther Point

GPIO Pin	Type	Default	FUNC/ TYPE	Usage	Pull up processing	Power	MUXED/ UNMUXED
GPIO 0	I/O	GPI	O	NC		+3.3V	
GPIO 1	I/O	GPI	O	PCH_SPIWP#	10K pull-up to +3V	+3.3V	
GPIO 2	I/O	GPI	I/OD	NC		+3.3V	
GPIO 3	I/O	GPI	I/OD	NC		+3.3V	
GPIO 4	I/O	GPI	I/OD	NC		+3.3V	
GPIO 5	I/O	GPI	I/OD	NC		+3.3V	
GPIO 6	I/O	GPI	O	GPIO6	4.7K pull-up to +3V	+3.3V	
GPIO 7	I/O	GPI	O	SIO_PME#	4.7K pull-up to +3V	3VSB	
GPIO 8	I/O	GPO	I	Internal 20K pull-up to +3VSB, 1k pull-down to GND		3VSB	UNMUXED
GPIO 9	I/O	Native	I	USB_OCP#5	10K pull-up to +3VSB	3VSB	
GPIO 10	I/O	Native	I	USB_OCP#6	10K pull-up to +3VSB	3VSB	
GPIO 11	I/O	Native	I	SMBALERT#		3VSB	
GPIO 12	I/O	Native	O	NC		3VSB	
GPIO 13	I/O	GPI	O	HDA_DOCK_RST#	Reserve 10K pull-up to +3VSB	3VSB	
GPIO 14	I/O	Native	I	USB_OCP#7	10K pull-up to +3VSB	3VSB	
GPIO 15	I/O	GPO	I	NC		3VSB	UNMUXED
GPIO 16	I/O	GPI	I	GPIO16	4.7K pull-up to +3V	+3.3V	
GPIO 17	I/O	GPI	I	DGPU_PWROK	10K pull-down to GND	+3.3V	
GPIO 18	I/O	Native	I	NA		+3.3V	
GPIO 19	I/O	GPI	I	BBS_BIT0	10K pull-up to +3V	+3.3V	
GPIO 20	I/O	Native	I	PCIECLKRQ2#	10K pull-up to +3V	+3.3V	
GPIO 21	I/O	GPI	I	GPIO21	10K pull-up to +3V	+3.3V	
GPIO 22	I/O	GPI	I	BIOS_REC	10K pull-up to +3V	+3.3V	
GPIO 23	I/O	Native	I	Test Point	Internal 20K pull-up to +3V	+3.3V	
GPIO 24	I/O	GPO	O	USB_EN	Reserve 10K pull-down to GND	3VSB	UNMUXED
GPIO 25	I/O	Native	I	PCIECLKRQ3#	10K pull-down to GND	3VSB	
GPIO 26	I/O	Native	I	PCIECLKRQ4#	10K pull-down to GND	3VSB	
GPIO 27	I/O	GPI	I	Test Point	+3VSB_DS	+3VSB_DS	UNMUXED
GPIO 28	I/O	GPO	O	PLL_ODVR_EN	Internal PU, Reserve 1K pull-down	3VSB	UNMUXED
GPIO 29	I/O	GPI	O	SLP_LAN#		3VSB	
GPIO 30	I/O	Native	O	SUSWARN#	Reserve 10K pull-up to +3VSB_DS +3VSB_DS	+3VSB_DS	
GPIO 31	I/O	GPI	I	ACPRESENT	10K pull-up to +3VSB_DS	+3VSB_DS	
GPIO 32	I/O	Native	I/O	PM_CLKRUN#	8.2K pull-up to +3V	+3.3V	UNMUXED
GPIO 33	I/O	GPO	I	Test Point		+3.3V	
GPIO 34	I/O	GPI	O	STP_PCI#	10K pull-up to +3V	+3.3V	
GPIO 35	I/O	GPO	I	DGPU_HPD_INTR#	10K pull-up to +3V	+3.3V	UNMUXED
GPIO 36	I/O	GPI	I	GPIO36	Reserve 200k pull-up to +3V	+3.3V	
GPIO 37	I/O	GPI	I	GPIO37	100K pull-down to GND	+3.3V	
GPIO 38	I/O	GPI	O	GPIO38	4.7K pull-up to +3V	+3.3V	
GPIO 39	I/O	GPI	I	CRB_SV_DET	10K pull-up to +3V	+3.3V	
GPIO 40	I/O	Native	I	USB_OCP#1	10K pull-up to +3VSB	3VSB	
GPIO 41	I/O	Native	I	USB_OCP#2	10K pull-up to +3VSB	3VSB	
GPIO 42	I/O	Native	I	USB_OCP#3	10K pull-up to +3VSB	3VSB	
GPIO 43	I/O	Native	I	USB_OCP#4	10K pull-up to +3VSB	3VSB	
GPIO 44	I/O	Native	I	PCIECLKRQ5#	10K pull-up to GND	3VSB	
GPIO 45	I/O	Native	I	NC	10K pull-up to +3VSB	3VSB	
GPIO 46	I/O	Native	O	NC	10K pull-up to +3VSB	3VSB	
GPIO 47	I/O	Native	I	PEG_CLKRQ#	Reserve 10K pull-down to GND	3VSB	
GPIO 48	I/O	GPI	O	GPIO48	4.7K pull-up to +3V	+3.3V	
GPIO 49	I/O	GPI	O	GPIO49	4.7K pull-up to +3V	+3.3V	
GPIO 50	I/O	Native	I	REQ1#	8.2K pull-up to +3V	+3.3V	
GPIO 51	I/O	Native	I	BBS_BIT1	Internal 20Kpull-up, Reserve 1K pull-down	+3.3V	
GPIO 52	I/O	Native	I	DGPU_SELECT#	8.2K pull-up to +3V	+3.3V	
GPIO 53	I/O	Native	O	DGPU_PWM_SELECT#	Internal 20Kpull-up	+3.3V	
GPIO 54	I/O	Native	O	DGPU_PWR_EN#	8.2K pull-up to +3V	+3.3V	
GPIO 55	I/O	Native	I	GNT#3	Internal 20Kpull-up	+3.3V	
GPIO 56	I/O	Native	I	NC		3VSB	
GPIO 57	I/O	GPI	O	Test Point	Connect to TPM	3VSB	UNMUXED
GPIO 58	I/O	Native	I/OD	SML1_CLK	2.2K pull-up to +3VSB	3VSB	

GPIO Pin	Type	Default	FUNC/ TYPE	Usage	Pull up processing	Power	MUXED/ UNMUXED
GPIO 59	I/O	Native	I	USB_OCP#0	10K pull-up to +3VSB	3VSB	
GPIO 60	I/O	Native	ODO	DRAMRST_CNTRL_PCH	1K pull-up to +3VSB	3VSB	
GPIO 61	I/O	Native	O	NC		3VSB	
GPIO 62	I/O	Native	O	NC		3VSB	
GPIO 63	I/O	Native	O	NC		3VSB	
GPIO 64	I/O	Native	I/O	Test Point	Internal 20Kpull-down	+3.3V	
GPIO 65	I/O	Native	O	CLK_48M_SIO	Internal 20Kpull-down	+3.3V	
GPIO 66	I/O	Native	O	Test Point	Internal 20Kpull-down	+3.3V	
GPIO 67	I/O	Native	I	DGPU_PRSENT#	Internal 20Kpull-down	+3.3V	
GPIO 68	I/O	GPI	O	NC	Internal 20K pull-up to +3V	+3.3V	
GPIO 69	I/O	GPI	O	NC	Internal 20K pull-up to +3V	+3.3V	
GPIO 70	I/O	Native	O	NC	Internal 20K pull-up to +3V	+3.3V	
GPIO 71	I/O	Native	O	NC	Internal 20K pull-up to +3V	+3.3V	
GPIO 72	I/O	Native	O	BATLOW#	10K pull-up to +3VSB	3VSB	
GPIO 73	I/O	Native	I	PCIECLKRQ0#	10K pull-up to +3VSB	3VSB	
GPIO 74	I/O	Native	ODO	SML1ALERT#	10K pull-up to +3VSB	3VSB	
GPIO 75	I/O	Native	I/OD	SML1_DATA	2.2K pull-up to +3VSB	3VSB	

DDR3 DIMM Configuration

DEVICE	ADDRESS	CLOCK
DIMM 1	00	M_A_CLK_DDR0/M_A_CLK_DDR#0 M_A_CLK_DDR1/M_A_CLK_DDR#1
DIMM 2	10	M_B_CLK_DDR0/M_B_CLK_DDR#0 M_B_CLK_DDR1/M_B_CLK_DDR#1

SMBus Distribution

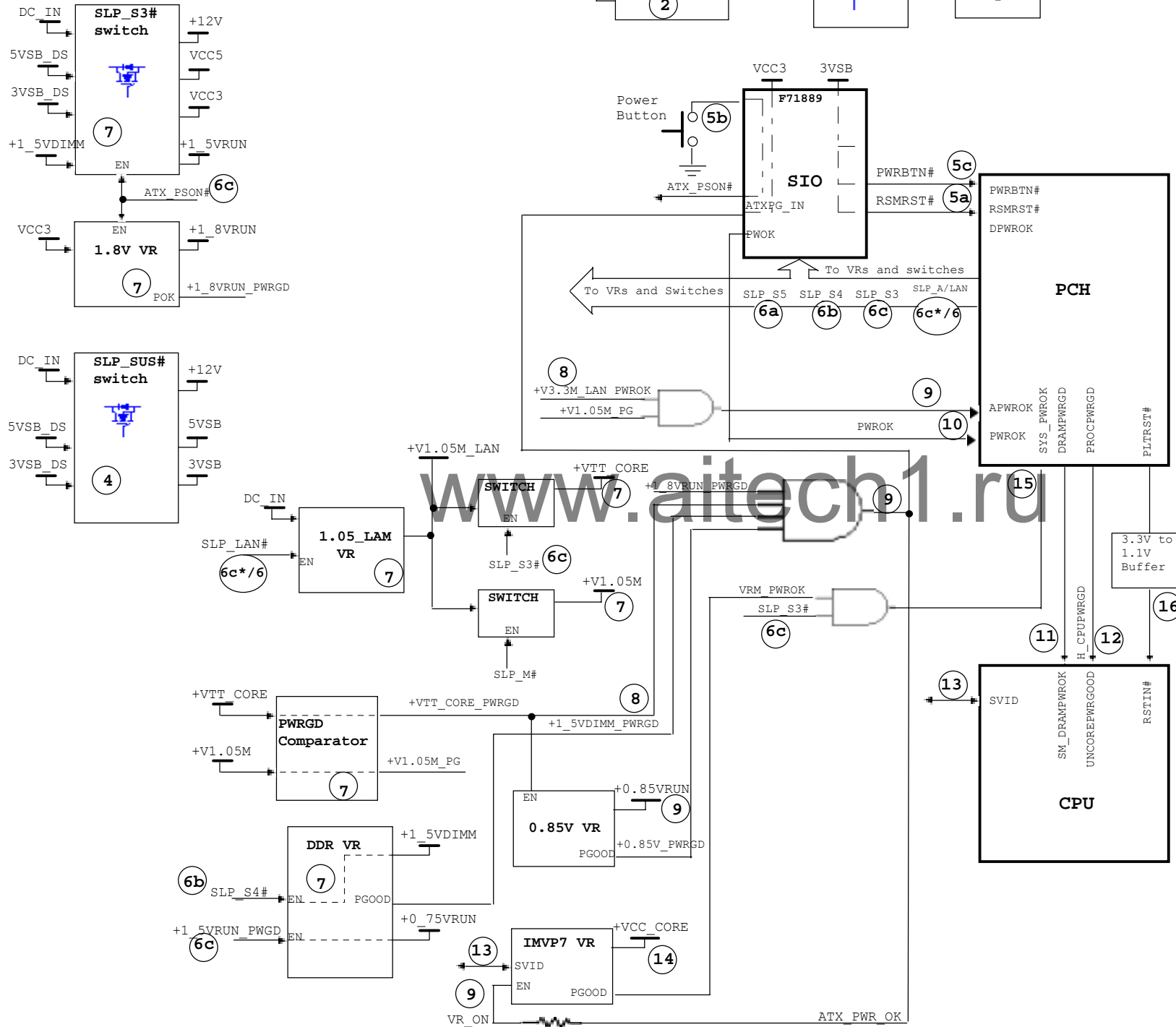
SMBus	Power	Load
SMBCLK_MAIN	VCC3	DIMM, Mini PCIE, PCIE X16, e-DP

Jumper Setting

J1	(1-2) 5V	(2-3) 12V, COM1 Voltage Select
J2	(1-2) 3V	(2-3) 5V, LVDS Voltage Select
JCMOS1	(1-2) Normal	(2-3) Clear CMOS
JCMV2	(1-2) 5V	(2-3) 12V, COM2 Voltage Select
JCMV3	(1-2) 5V	(2-3) 12V, COM2 Voltage Select
JCMV4	(1-2) 5V	(2-3) 12V, COM2 Voltage Select
JATX1	(1-2) ATX	(2-3) AT

msi			
Title			
GPIO PIN Definitions/Config			
Size	Document Number	Rev	
Custom	MS-9899	10	
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Power up Sequence Diagram



SIO F81866D

GPIO Pin	Type	Default	FUNC/ TYPE	Usage	Pull up processing	Power	NOTE
GPIO 0	I/O	Native	OD	NC		3VSB	
GPIO 01	I/O	Native	OD	NC		3VSB	
GPIO 02	I/O	Native	I	SUSWARN#_SIO		3VSB	
GPIO 03	I/O	Native	OD	SUSACK#_SIO		3VSB	
GPIO 04	I/O	GPI	OD	SLP_SUS#_SIO		3VSB	
GPIO 05	I/O	GPI	OD	NC		3VSB	
GPIO 06	I/O	Native	I/OD	NC		3VSB	
GPIO 07	I/O	Native	OD	NC		3VSB	
GPIO 10	I/O	Native	I/OD	LED_VSB#		3VSB	
GPIO 11	I/O	Native	OD	LED_VCC#		3VSB	
GPIO 12	I/O	GPI	I/OD	USB3_EN		3VSB	
GPIO 13	I/O	Native	I/OD	EN232_L		3VSB	
GPIO 14	I/O	Native	I/OD	ATX_AT_TRAP		3VSB	
GPIO 15	I/O	Native	I/O	WDTO#	10K pull-up to 3VSB	3VSB	
GPIO 16	I/O	Native	OD	SIO_SDA0		3VSB	
GPIO 17	I/O	Native	I/OD	PECI_SIO	100K pull-down to GND	3VSB	
GPIO 20	I/O	Native	I/OD	SIO_SCL0		3VSB	
GPIO 21	I/O	Native	I	ATX_PWR_OK	4.7K pull-up to +3V	3.3V	
GPIO 22	I/O	Native	I	PSIN#		3.3V	
GPIO 23	I/O	Native	I	PM_PWRBTN#		3.3V	
GPIO 24	I/O	Native	O	SLP_S3		3.3V	
GPIO 25	I/O	Native	O	PS_ON#		3.3V	
GPIO 26	I/O	Native	I	PWOK	4.7K pull-up to +3V	3.3V	
GPIO 27	I/O	Native	O	RSMRST#		3.3V	
GPIO 50	I/O	Native	I	W_DISABLE1#		3.3V	
GPIO 51	I/O	Native	I	PWM_FAN_EN		3.3V	
GPIO 52	I/O	Native	I	NC		3.3V	
GPIO 53	I/O	Native	I	#EN485		3.3V	
GPIO 54	I/O	Native	I	#EN422		3.3V	
GPIO 55	I/O	Native	O	NC		3.3V	
GPIO 56	I/O	Native	O	NC		3.3V	
GPIO 57	I/O	Native	O	NC		3.3V	
GPIO 60	I/O	Native	O	NC		3.3V	
GPIO 61	I/O	Native	I	NC		3.3V	
GPIO 62	I/O	Native	I	NC		3.3V	
GPIO 63	I/O	Native	I	NC		3.3V	
GPIO 64	I/O	Native	I	NC		3.3V	
GPIO 65	I/O	Native	I	SIO_PME#	4.7K pull-up to 3VSB	3VSB	
GPIO 66	I/O	Native	I	DPWROK_SIO		3.3V	
GPIO 67	I/O	Native	I	SLP_S4#		3.3V	
GPIO 70	I/O	Native	I/O	SIO_GPIO70		3.3V	GPO
GPIO 71	I/O	Native	I/O	SIO_GPIO71		3.3V	GPO
GPIO 72	I/O	Native	I/O	SIO_GPIO72		3.3V	GPO
GPIO 73	I/O	Native	I/O	SIO_GPIO73		3.3V	GPO

GPIO Pin	Type	Default	FUNC/ TYPE	Usage	Pull up processing	Power	NOTE
GPIO 74	I	Native	I/O	SIO_GPIO74		3.3V	GPI
GPIO 75	I	Native	I/O	SIO_GPIO75		3.3V	GPI
GPIO 76	I	Native	I/O	SIO_GPIO76		3.3V	GPI
GPIO 77	I	Native	I/O	SIO_GPIO77		3.3V	GPI
GPIO 80	OD	Native	I/O	NC		3.3V	
GPIO 81	OD	Native	I/O	NC		3.3V	
GPIO 82	OD	Native	I/O	NC		3.3V	
GPIO 83	OD	Native	I/O	NC		3.3V	
GPIO 84	OD	Native	I/O	NC		3.3V	
GPIO 85	OD	Native	I/O	NC		3.3V	
GPIO 86	OD	Native	I/O	NC		3.3V	
GPIO 87	OD	Native	I/O	NC		3.3V	

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Version 1.0

DDR3 support low voltage
DDR3 added Vref DQ from CPU to DDR DQ voltage
added DPLL_ref_clk to PCH for eDP

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